CMS Pixel Chip PSI46 V2
- preliminary tests -

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PSI46V2 Test procedure

The test procedure is identical with V1 testing in November 2004 :

- Set interface board I2C address (adrsl), calibrate pulse number (ncal), trigger pulse number (ntrig), token delay (tokendel), PSI46 and I2C frequency (freq) and I2C clock to 'external'. These parameters are not changed during test.
- Load interface board FIFOs with
  - a) PSI46 DAC settings (suggested values from PSI) and
  - b) program data for all pixels in 'unmask' mode (pixel enabled) with trim=8 (0 to 16)
- Set programmable power supply ON (psdig~2.5V, psana~1.5V) and do chip reset
- Read power supply currents and voltages (first time)
- Start FIFO stream download to PSI46
- Read power supply currents and voltages (second time)
- Issue a single trigger sequence, do timing reset and do clear calibration (clears all pixels data)
- Test DACs' linearity for six values: use 0x00,40,80,C0,FF and default for 8bit DACs, use 0x00,4,8,C,F and default for 4bit DACs
- Start a pixel cycle, which includes scanning VCAL and trim bits between some minimum and maximum values. Only one pixel at a time is calibrated and measured. First set mask=1 (pixel enabled) and trim bits to a minimum value. Increase VCAL until pixel responds. Store this data. Flag if more than one pixel is responding. Set VCAL to maximum and disable pixel. Verify that pixel is not responding. Enable again the pixel and increment trim bits. Repeat VCAL cycle. When done with all trim bits, go to next pixel and repeat. Do this for all 52*80 pixels.
- Set programmable power supply OFF
- Start data_analysis program and write report file

PSI46 DACs' Linearity test

****
REPORTING DAC LINEARITY TEST RESULTS
****

DAC(dec)	DAC(hex)	Slope	Intercept	RSQ	MIN(%)	MAX(%)
1	1	0	0	0	0	0
2	2	0	0	0	0	0
3	3	-2.33	2695	-1	-0.39	0.33
4	4	-38.03	2668	-1	-0.39	0.28
5	5	-2.33	2693	-1	-0.35	0.4
6	6	-37.55	2657	-1	-0.25	0.27
7	7	-2.33	2691	-1	-0.33	0.26
8	8	-37.46	2657	-1	-0.35	0.41
9	9	-2.32	2693	-1	-0.32	0.27
10	A	-2.34	2698	-1	-0.39	0.28
11	B	-2.35	2699	-1	-0.45	0.26
12	C	-2.38	2707	-1	-0.43	0.28
13	D	-2.3	2687	-1	-0.4	0.26
14	E	-37.41	2657	-1	-0.32	0.27
15	F	-2.23	2667	-1	-0.26	0.31
16	10	-2.24	2666	-1	-0.28	0.17
17	11	-2.24	2669	-1	-0.4	0.26
18	12	-2.23	2668	-1	-0.31	0.32
19	13	-0.1	2237	-0.08	-6.76	5.27
20	14	-2.37	2703	-1	-0.38	0.28
21	15	-0.01	2266	-0.01	-7.92	5.65
22	16	-2.41	2719	-1	-0.44	0.31
23	17	-2.39	2712	-1	-0.41	0.53
24	18	-2.38	2711	-1	-0.46	0.51
25	19	-2.32	2678	-1	-0.34	0.24
26	1A	-2.31	2675	-1	-0.43	0.4
27	1B	-1.04	2503	-0.71	-6.97	6.23
28	FE	-0.04	3136	-0.49	-0.39	0.17
29	FD	0	0	0	0	0

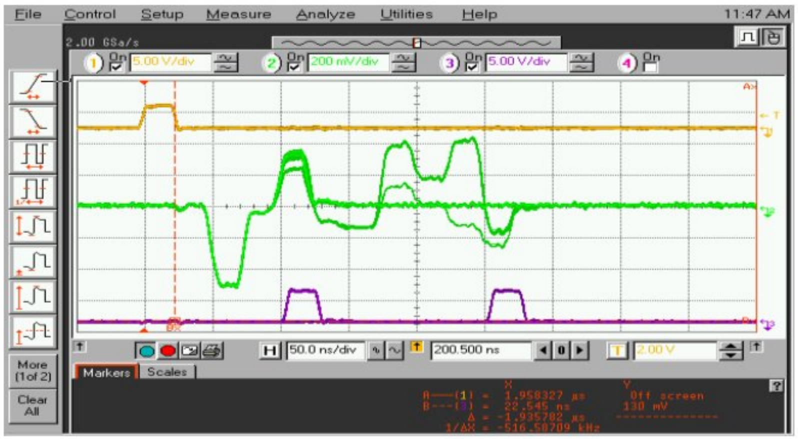
****
FAIL DACadd(dec)=19, error in DACLinMinDev = -6.76% < -1%
FAIL DACadd(dec)=19, error in DACLinMaxDev = 5.27% > 1%
FAIL DACadd(dec)=21, error in DACLinMinDev = -7.92% < -1%
FAIL DACadd(dec)=21, error in DACLinMaxDev = 5.65% > 1%
FAIL DACadd(dec)=27, error in DACLinMinDev = -6.97% < -1%
FAIL DACadd(dec)=27, error in DACLinMaxDev = 6.23% > 1%
****

- Each DAC data is interpolated with a straight line.
- The report file shows the DAC address (in hex), the SLOPE and INTERCEPT of the fit-line (in ADC counts), a statistical indication of linearity (RSQ is the Pearson product momentum correlation coefficient) and the minimum and maximum deviation of measured point from fit-line (in percentage).
- There is also a PASS/FAIL report based on a +-1% deviation from the fit-line. Also, if the pixel response has more 'bits' than UltraBlack, Black and LastDac, a DACLinLength error is reported.
- The DACs that control the power supply regulators of the chip (0x01 and 0x02) are not investigated.

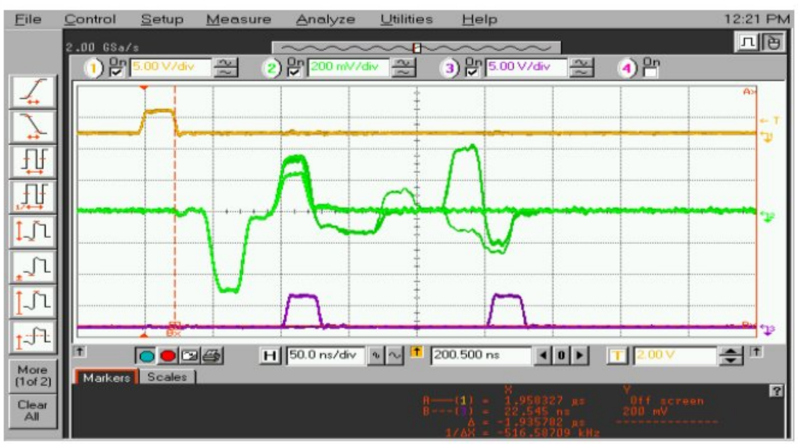
Comments:

- For unknown reasons, Vbias_ph (0x13) and Vbias_roc (0x15) controlling the chip readout analog levels have higher nonlinearity. This was observed also on V1 chip.
- The RangeTemp(0x1B) nonlinearity is 'normal' and was investigated in V1 study (see November 2004 report)

Multiple hit problem (power supply)

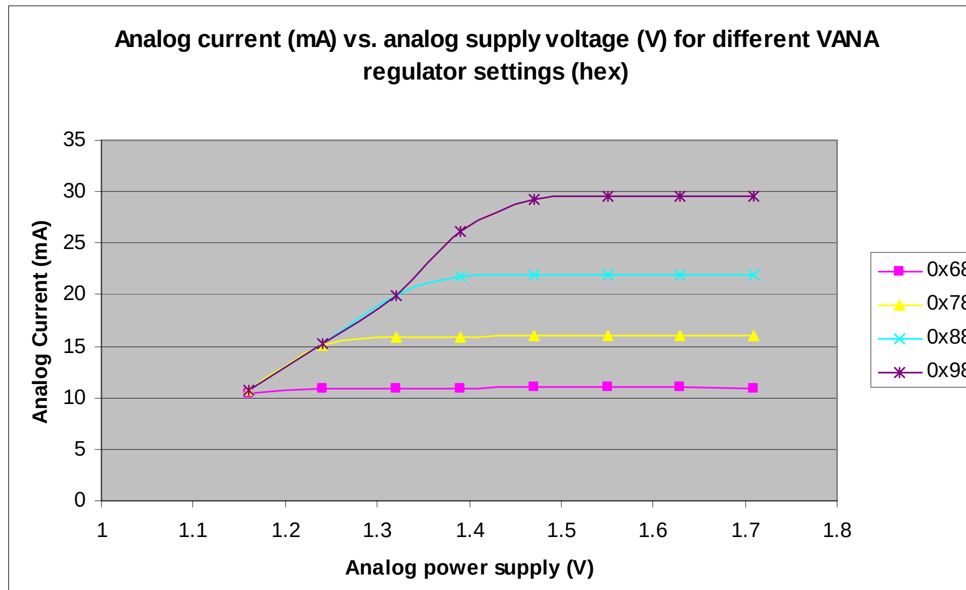


One pixel cell (pc=Gx0, pr=Gx0) showing two types of responses. The column address is the same,but row address is changed, being either pr=Gx0(4,2,4) or pr=Gx3D=dec41(2,1,0). No multiple hits observed (40MHz, internal CLK).



One pixel cell (pc=Gx0, pr=Gx25=dec57) showing two types of responses. The column address is the same,but row address is changed, being either pr=Gx25=dec57(1,1,4) or pr=Gx3D=dec41(2,1,0). No multiple hits observed (40MHz, internal CLK).

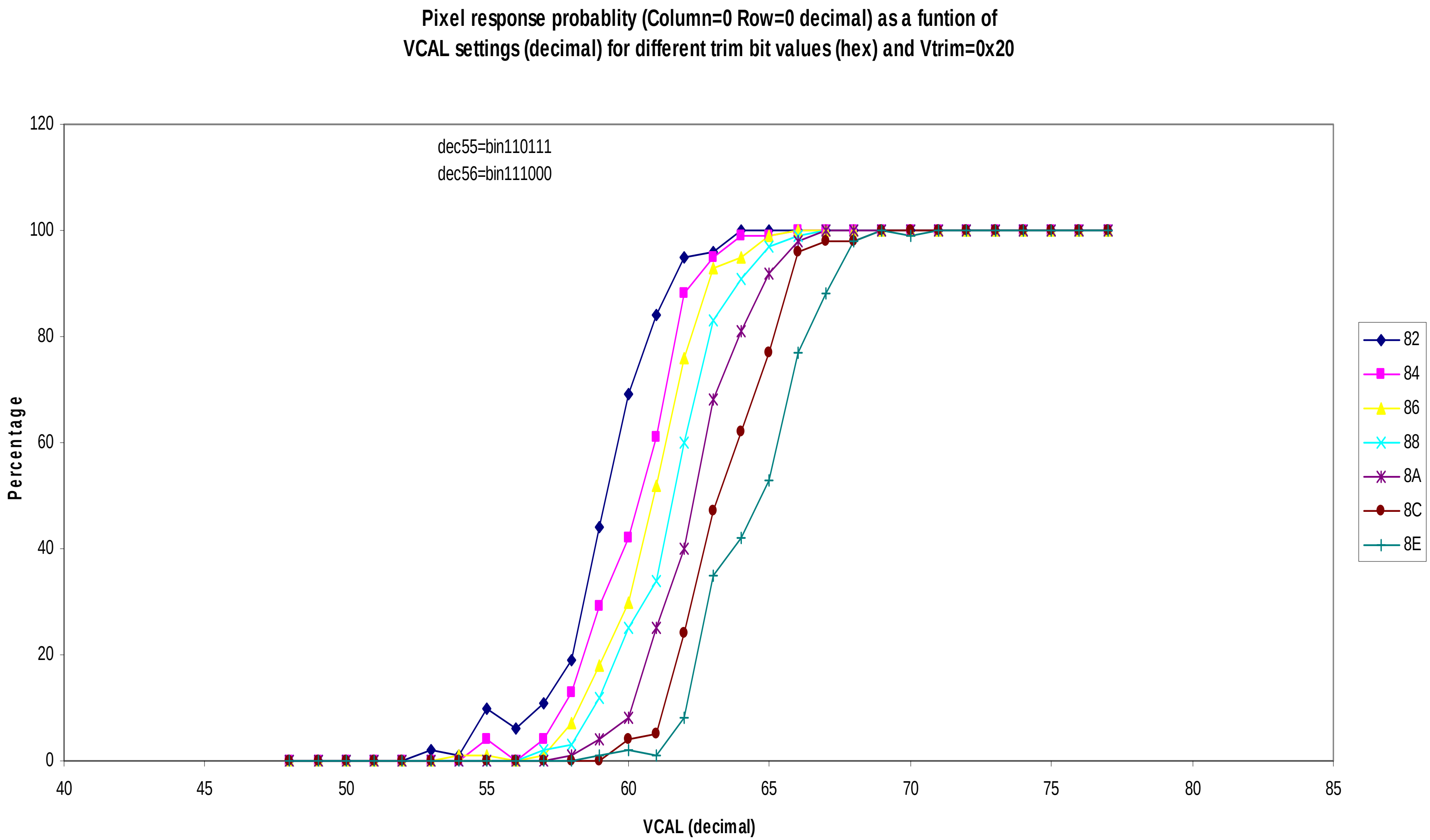
- The main issue we faced with V2 testing was the multiple hit problem, i.e. we calibrate and inject only one pixel, but more pixels are seen in the read-out (see left pictures).
- We thought first that the power supply voltages have not the necessary values (V1 didn't worked but for Vdig ~2V) so we did investigate the chips' power regulators influence (see below) on overall chip functionality/stability.
- There is no official specification. Eventually, after discussion with Roland H. we learned that their testing strategy includes a scan of Vana to determine a setting for which Iana~24mA. We didn't implemented this approach.



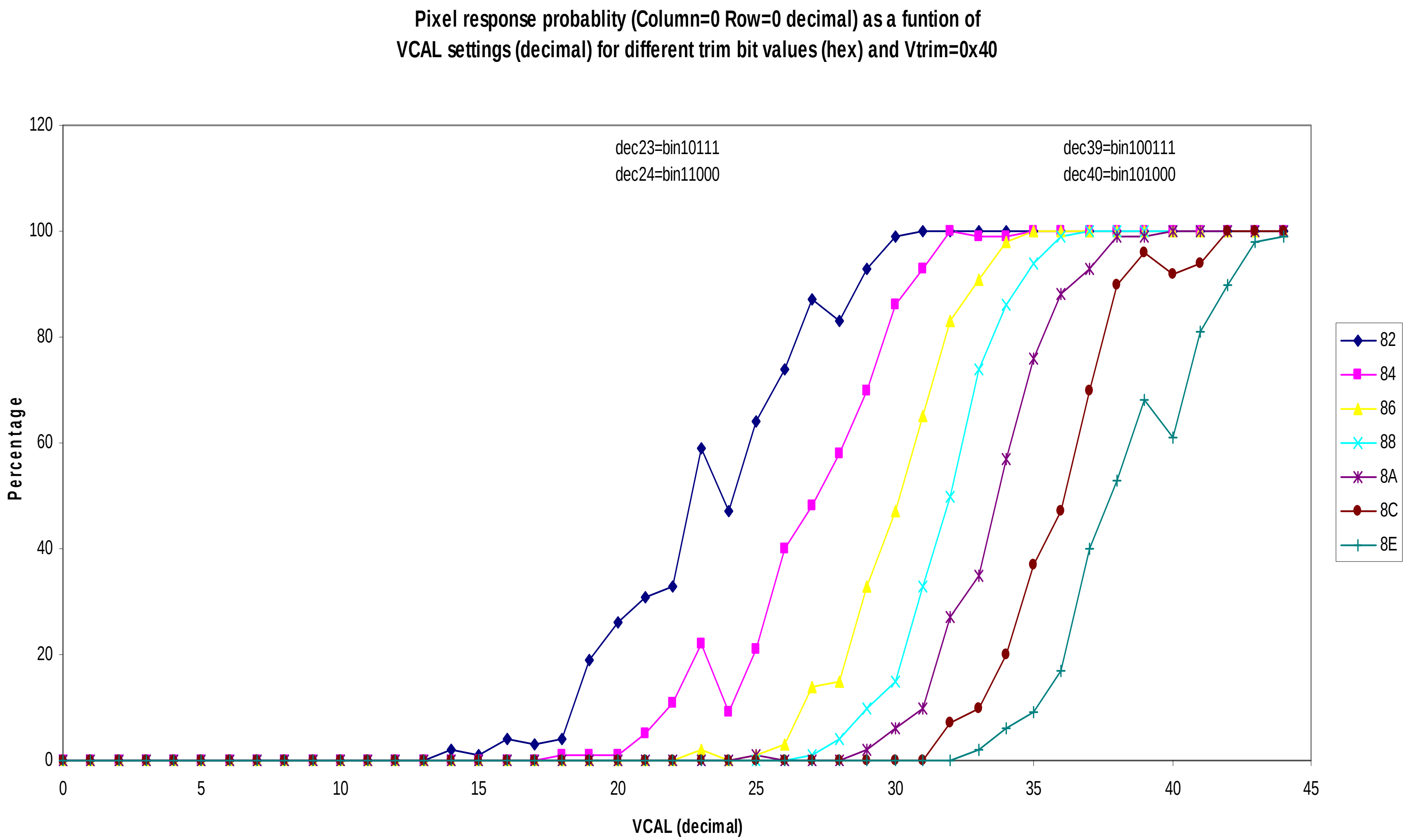
Pixel response dependence on Vtrim

- The following slides (6,7 and 8) show one pixel measured 100 times (see also November 2004 report). The Vtrim is 0x20, 0x40, 0x60 respectively and pixel response probability is plotted as VCAL increases, for different trim bits settings. The effect of Vtrim, in extending the 'sensitivity' range of the VCAL value where the pixel fires, can be easily seen in these slides.
- Note that comparing with similar measurements on V1, the response slope seems to be lower, which may be due to design changes in the injection circuit. Also like in V1 case, the same nonlinearities due to VCAL D/A converter can be seen when digital bits switch from, say 10111 to 11000.
- When Vtrim has quite high settings, say 0xD0 as in slide 9, the pixel shows a response only for trim bits 0x8C and 0x8E i.e. trim bits almost inactive (NOTE: the trim bits are 'active zero' so 0x8E means only the LSB is activated). So, in order to 'see' response when we increase the pixel threshold (by decreasing the trim setting to 0x8A, 0x88,… 0x82) we changed the settings as in slide 10: the VCAL range was increased from 280mV to 1800mV (using the new control bit from CTRL register) and the comparator threshold for all pixels (VthComp) was increased (VthComp setting decreased from 0x64 to 0x01).

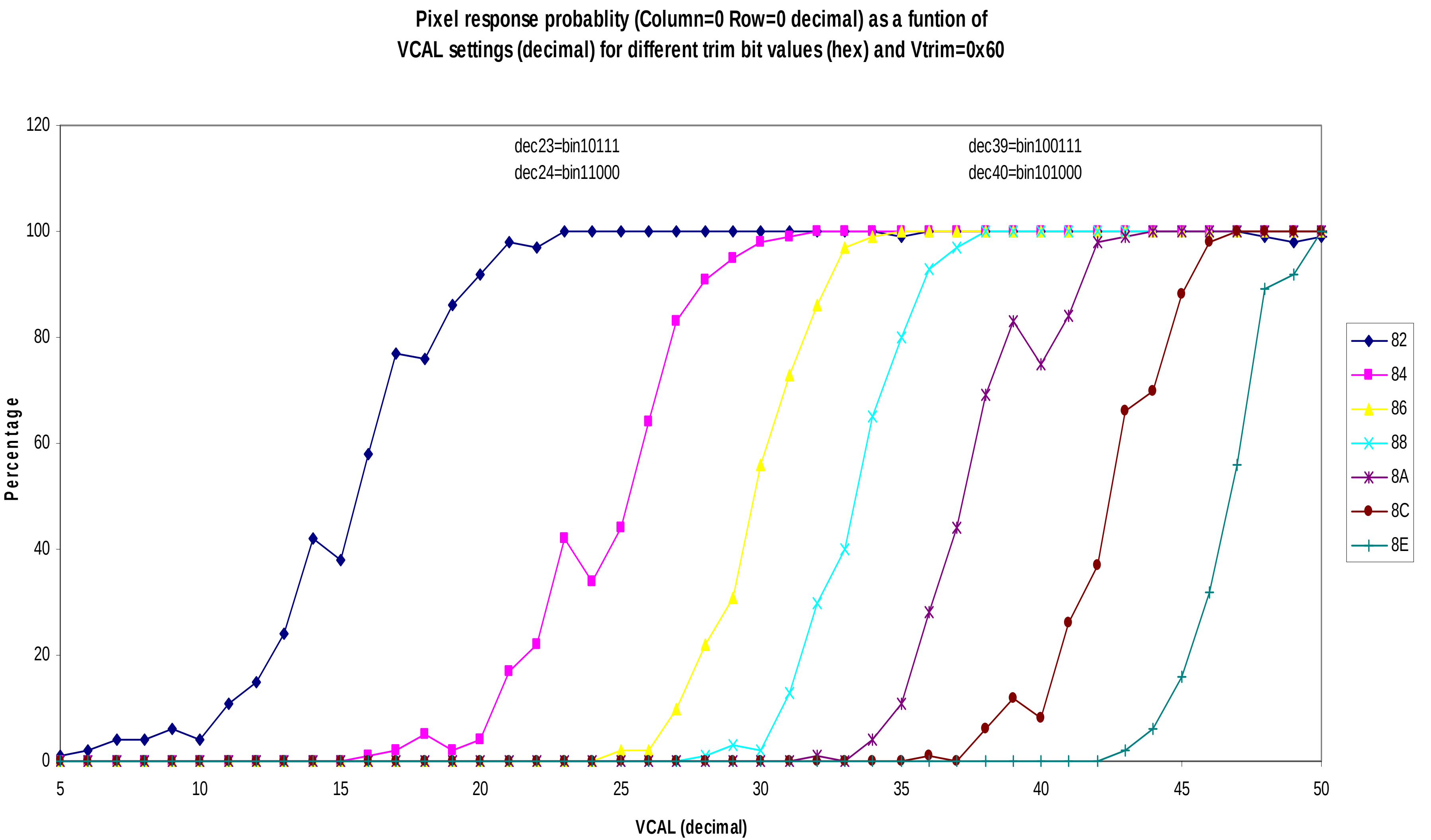
Pixel response dependence on Vtrim



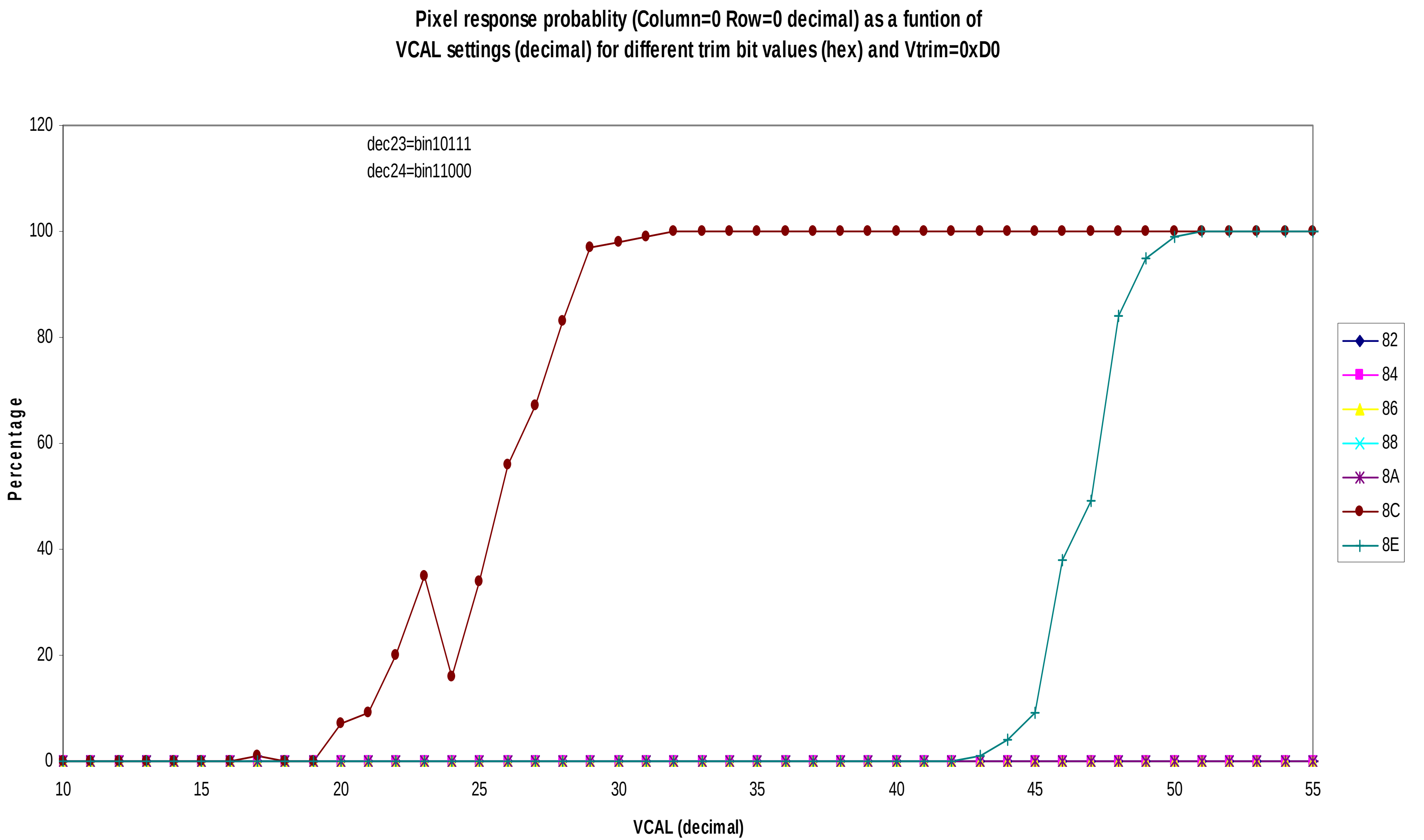
Pixel response dependence on Vtrim



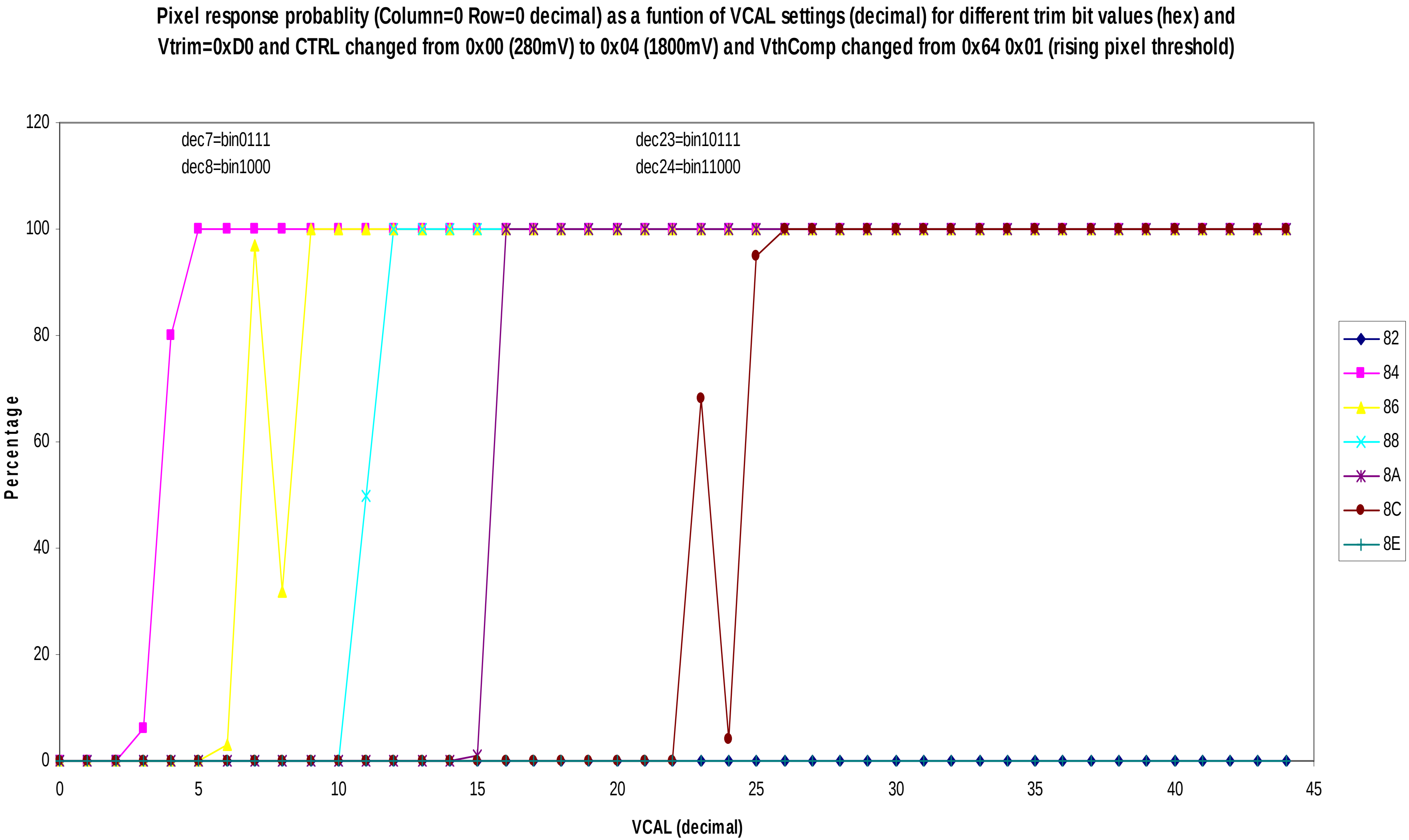
Pixel response dependence on Vtrim



Pixel response dependence on Vtrim



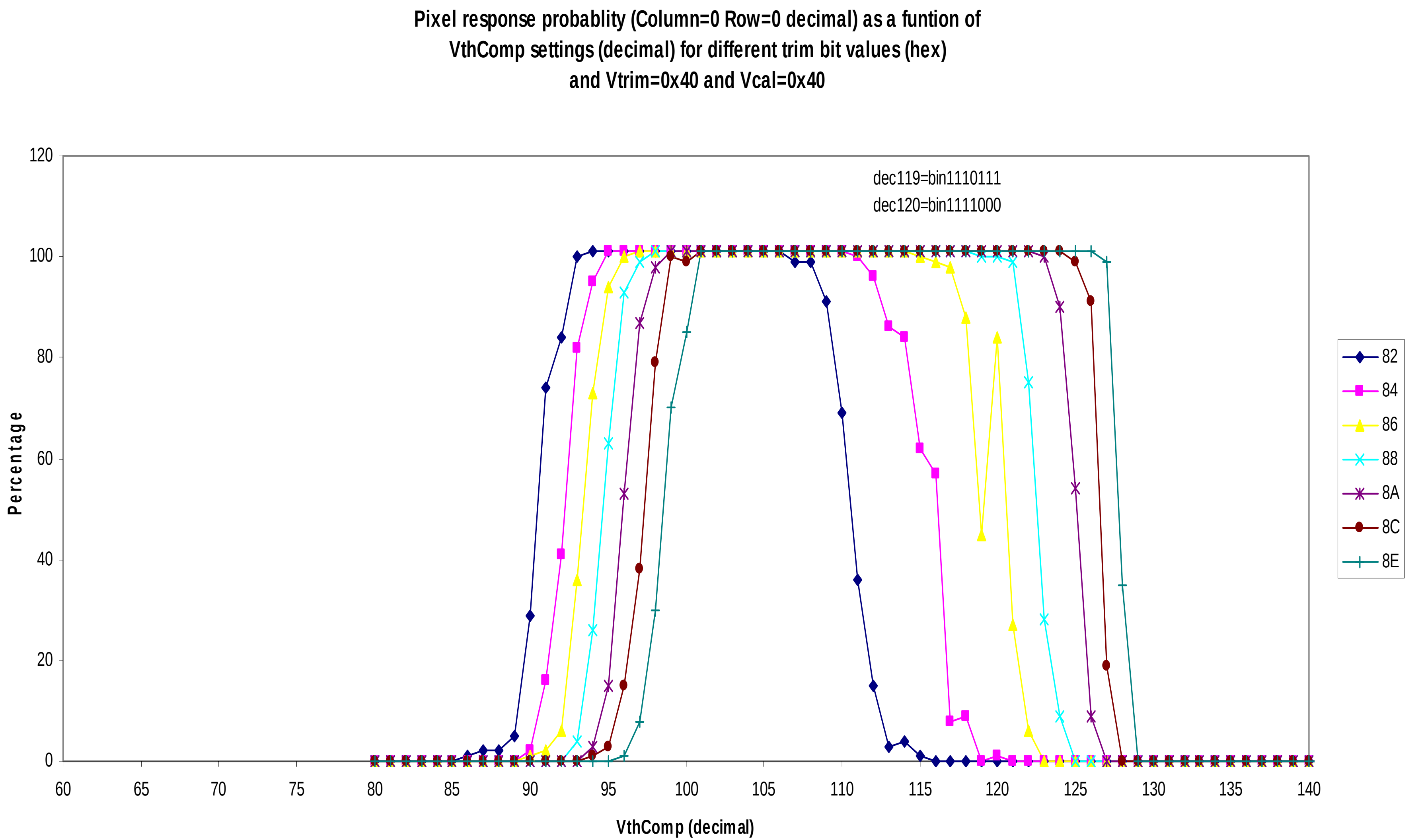
Pixel response dependence on Vtrim



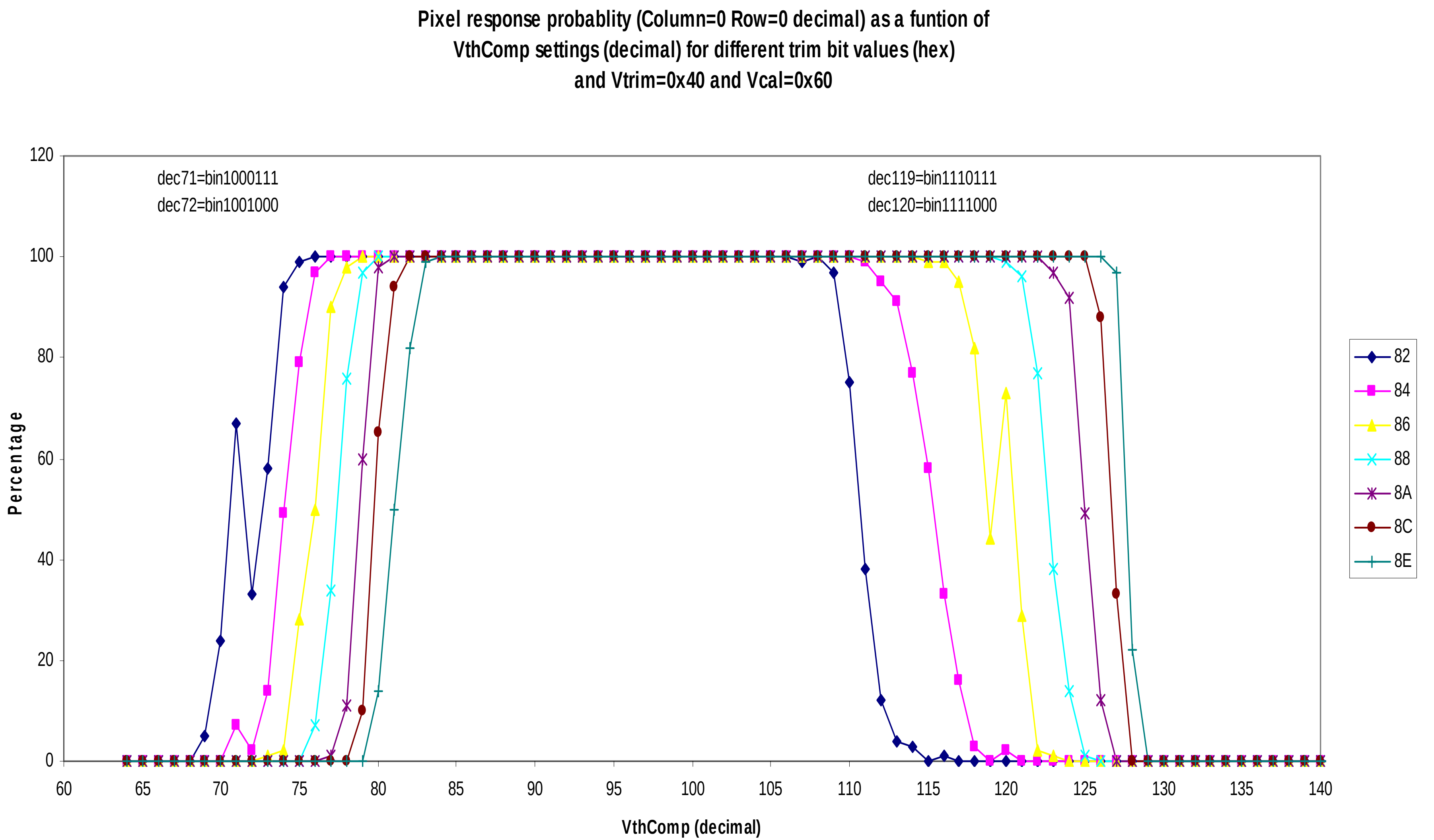
Pixel response dependence on VthComp

- Like the trim register Vtrim, the comparator threshold register VthComp is another register common for all pixels and acting at the pixel unit cell level. A third register that will be addressed later in a readout charge linearity study is the sample and hold delay register VHlddel.
- The VthComp effect on pixel's response, over 100 triggers is presented in the next four slides (12,13,14and 15), for all VCAL and VTRIM settings' combinations of 0x40 and 0x60.
- First we note again the same curve brake when digital bits switch from, say 10111 to 11000, this time for the VthComp D/A converter. It is likely that all the other registers' D/A converters have the same problem.
- Second, we observe that the pixel response curve with VthComp is a 'window' type response. This is OK and will be explained shortly.
- Third, if we compare graphs with the same Vtrim, we see that an increase in VCAL setting (i.e. an increase in the injected voltage) translates in the pixel firing at lower VthComp settings, i.e. higher comparator values. This is good behavior.
- Fourth, if we compare graphs with the same VCAL, we see that an increase in Vtrim setting translates in the pixel family of curves having wider window widths and being more apart each other. This is also a good behavior.
- Now, the falling edge of the window is due to the following effect: as VthComp setting increases the comparator value is decreased and all the pixels becomes more and more sensitive. At a certain moment, the noise limit is reached and, very quickly, all double column data buffers and/or time stamp buffers are occupied. There at least two ways to "catch" noisy pixels. In a discussion with Roland H. he suggested to enable more than one pixel, say two, but calibrate only one of them and look at the readout when VthComp is around the falling edge of the response window. While I perfectly agree with this approach, I couldn't do it because the multiple hit problem (see slide 16 with two oscilloscope pictures that show exactly my test pixel (0,0) and the two extra pixels (0,1) and (0,2) that are only enabled and not calibrated).
- So, I took another approach, which consists in the same enabling and calibrating only one pixel, but doing the readout on some other WBC number, up and down from the one in which I'm injecting. We can see in slide 17 that there are some pixels responses exactly on the window's falling edge.

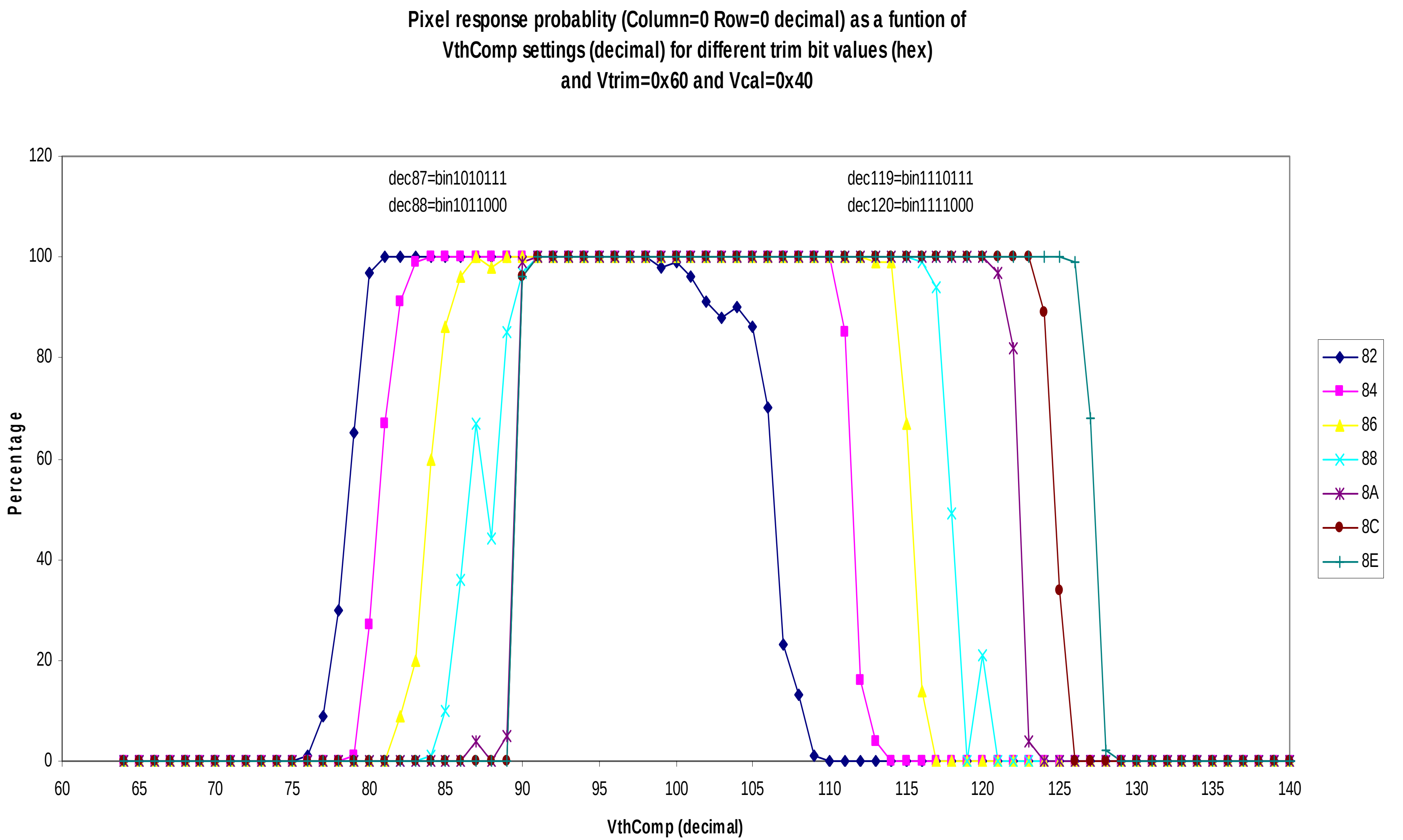
Pixel response dependence on VthComp



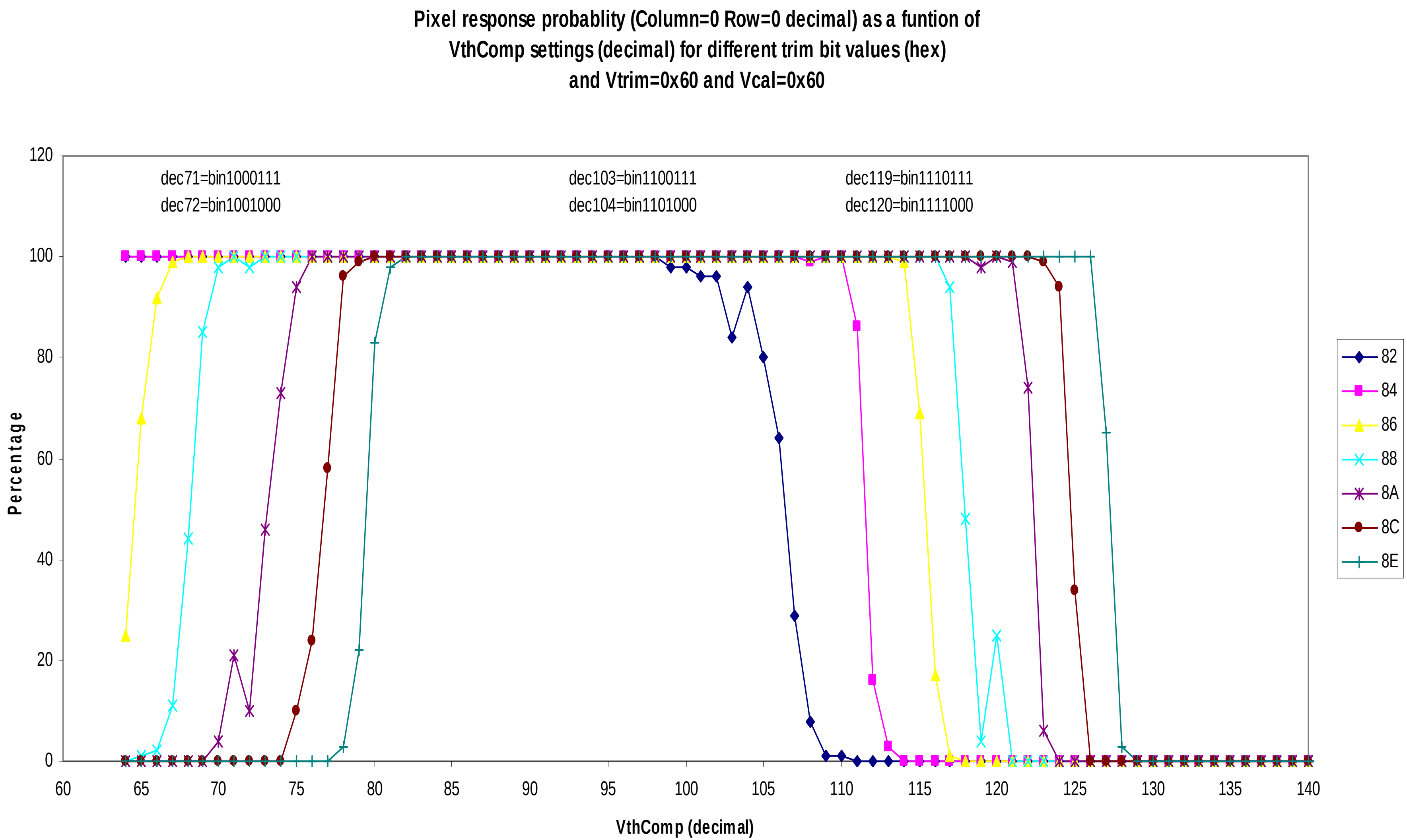
Pixel response dependence on VthComp



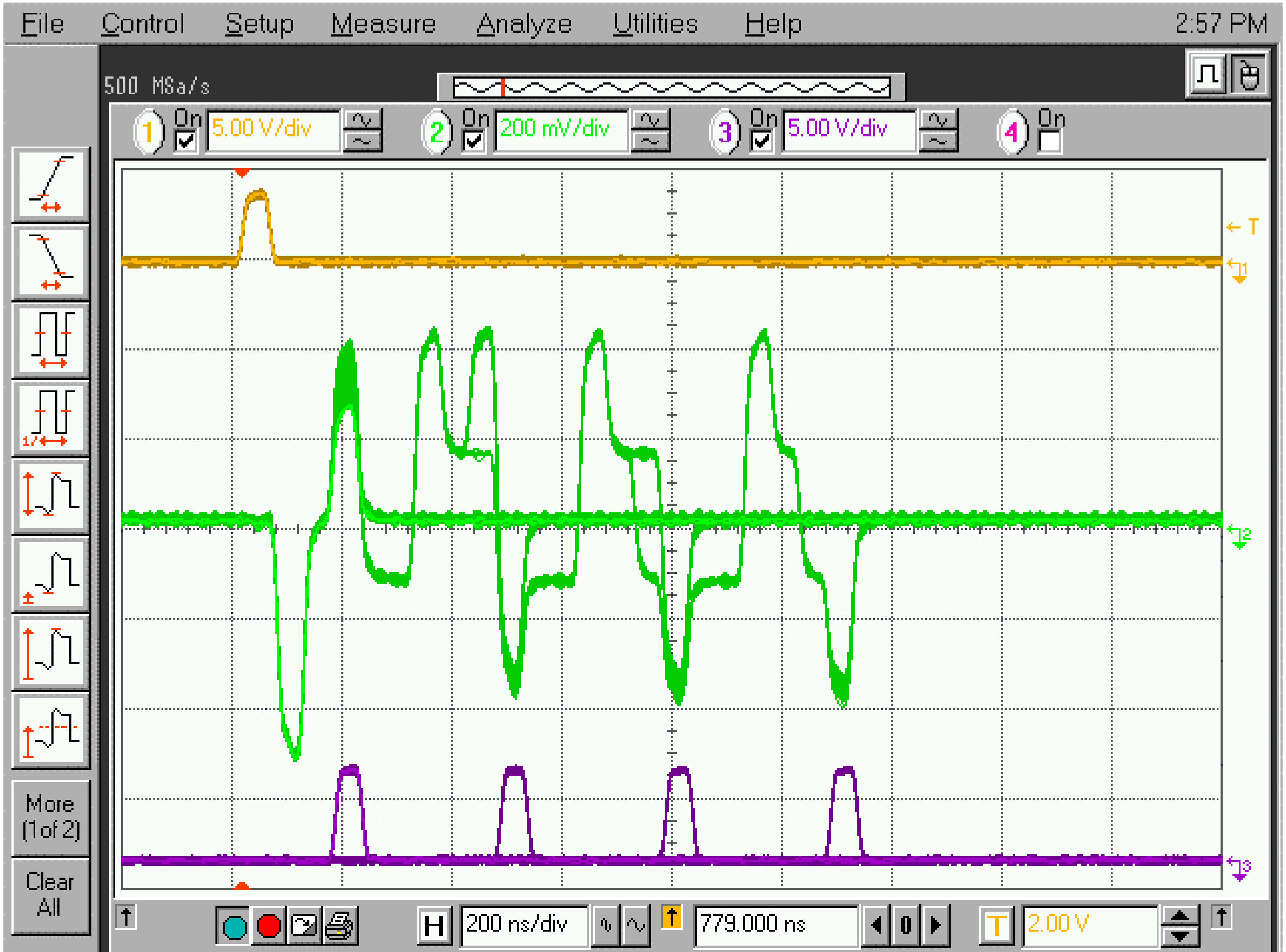
Pixel response dependence on VthComp



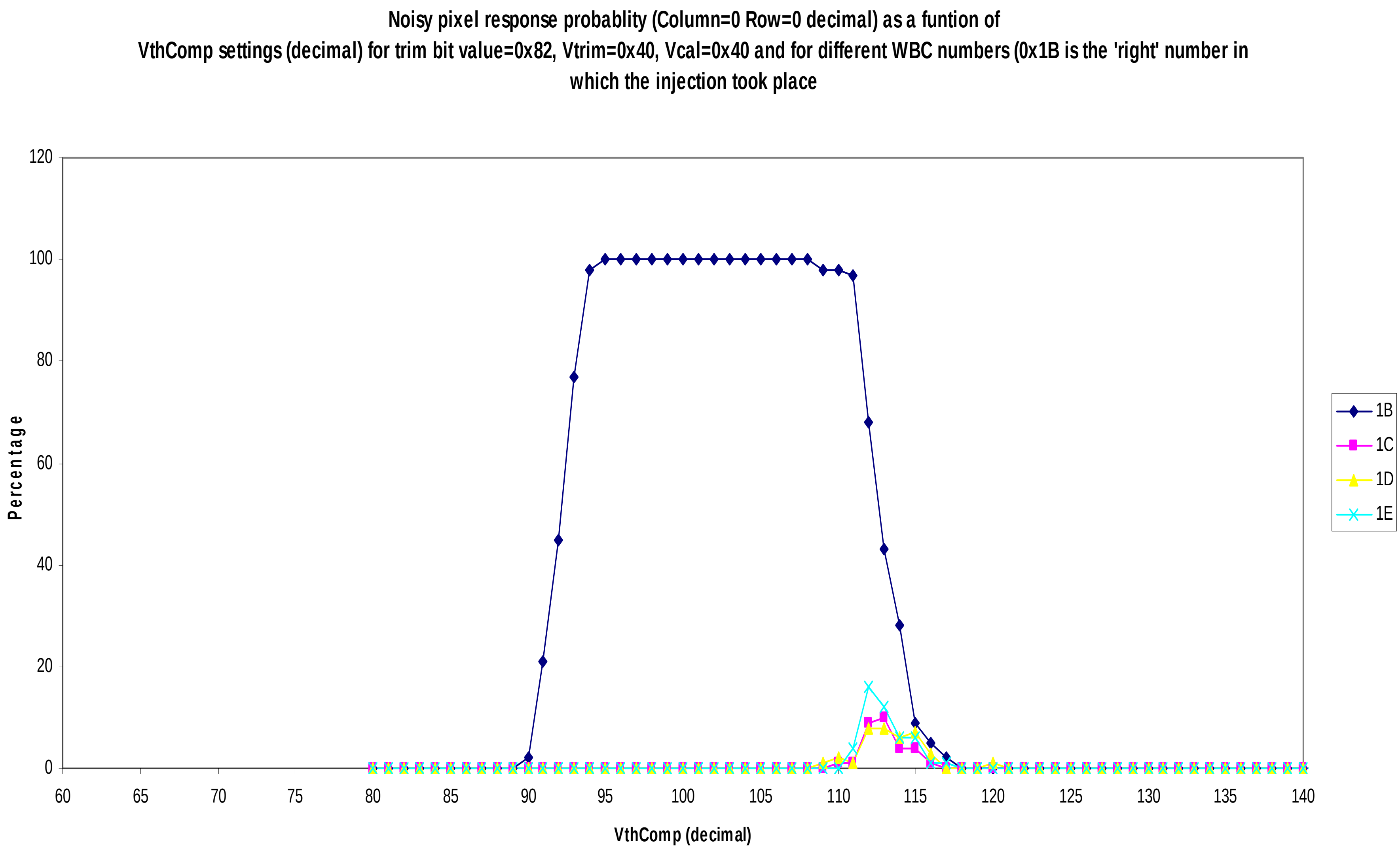
Pixel response dependence on VthComp



Pixel response dependence on VthComp



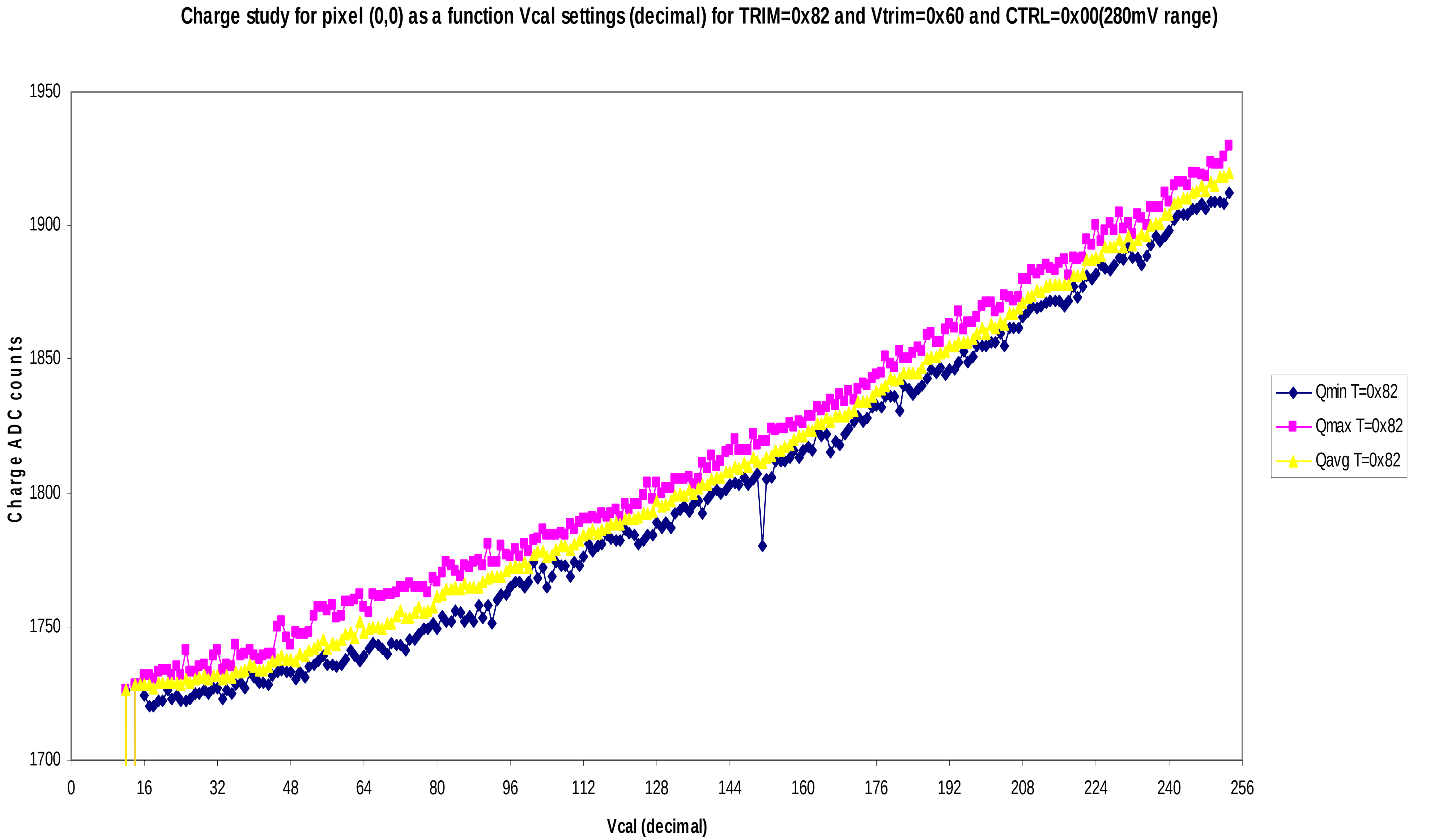
Pixel response dependence on VthComp



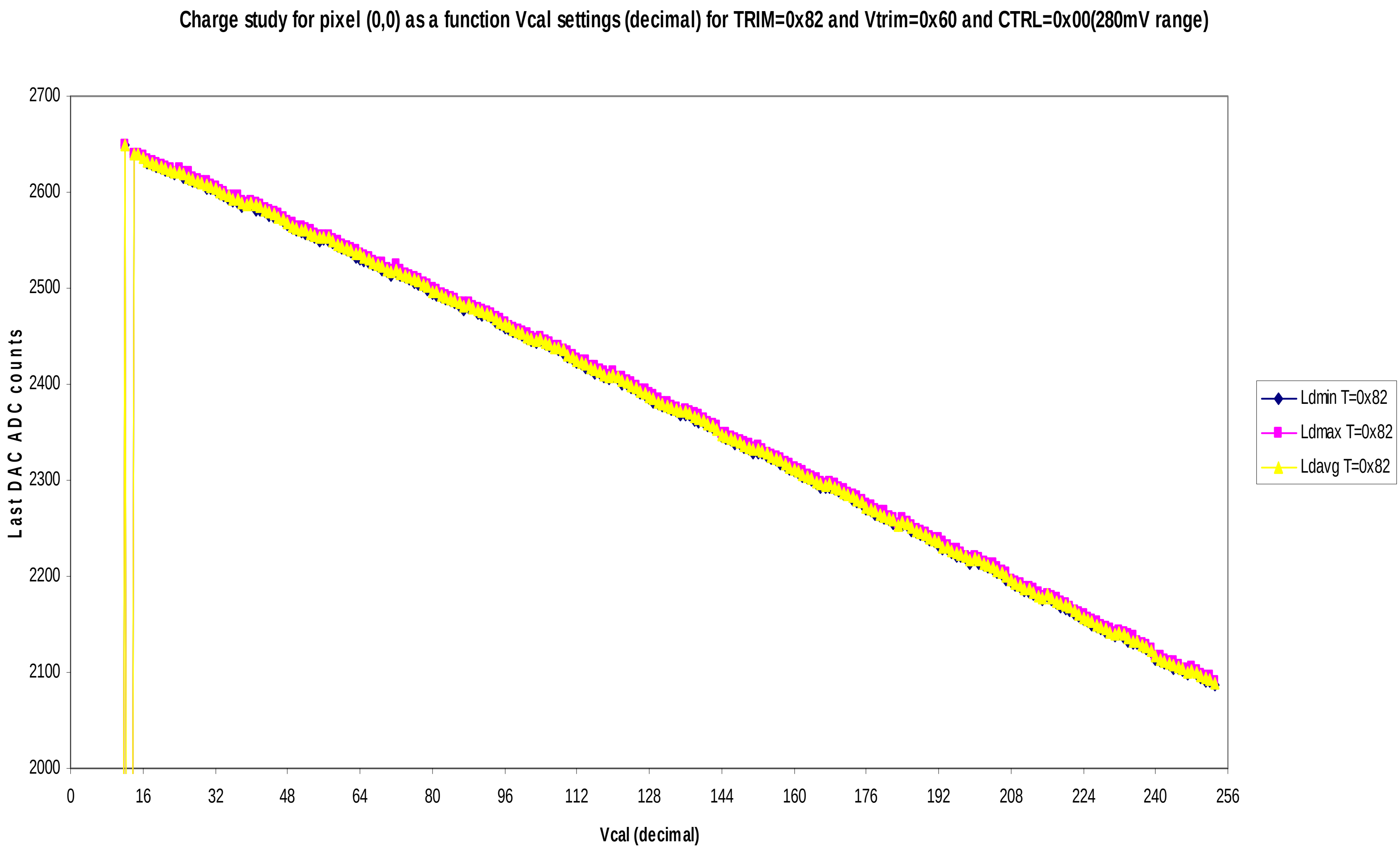
Pixel's charge dependence

- The pixel's readout charge was not investigated in V1 due to a design error that made the readout irrelevant.
- For this new V2 I started to investigate the charge linearity on VCAL for the small range (CTRL=0x04 <-> 280mV). The statistic is the same 100 triggers per pixel measurement conditions.
- Slide 19 to 24 show different charge readout plots for the VCAL range 280mV.
- The charge analog readout linearity in slide 19 seems to be reasonable (although I don't have a specification). The charge variation range over the 100 triggers seems to be, maybe, a little higher than expected (but also no specification available) – more on slide 21.
- Slide 20 shows the same dependence on VCAL settings for the 'LastDac' analog readout. While the linearity seems to be better, the now known curve break is visible (see blowup in slide 23).
- Slide 21 shows the variation range for the 100 triggers in a measurement. This range cumulates the chip contribution and the testing hardware contribution (which is a few counts). The charge range is clearly higher than the LastDac range (which is similar with the UltraBlack, Black and pedestal ranges). Again, I don't have an acceptance criteria.
- Slide 22 shows charge vs. LastDac readings (VCAL eliminated).
- Slide 24 shows the charge dependence for the large range (CTRL=0x00 <-> 1800mV). For reference purpose only, the 280mV range is also plotted. A saturation curve was noticed. Rolland H. suggests that it may be controlled by setting different values for the shaper regulators VrgSh and VwllSh. I used their suggested settings and I haven't had time to investigate this dependence further.
- On the other hand, it seems that trim bits settings is affecting somehow the readout charge, as shown in slide 25. Ideally the readout charge should not depend on pixel trim bits settings, but slide 25 suggest it does somehow. Rolland H. advised to change VthComp and VHldDel. Changing hold delay register, up and down from the suggested 0x58, as shown in slide 26, did not solve the problem. I haven't tried to change the other register, but if this variation of charge readout with trim bits is not acceptable we need to understand and correct it. I also have no idea how stable is the readout charge is some other DAC settings are changed.

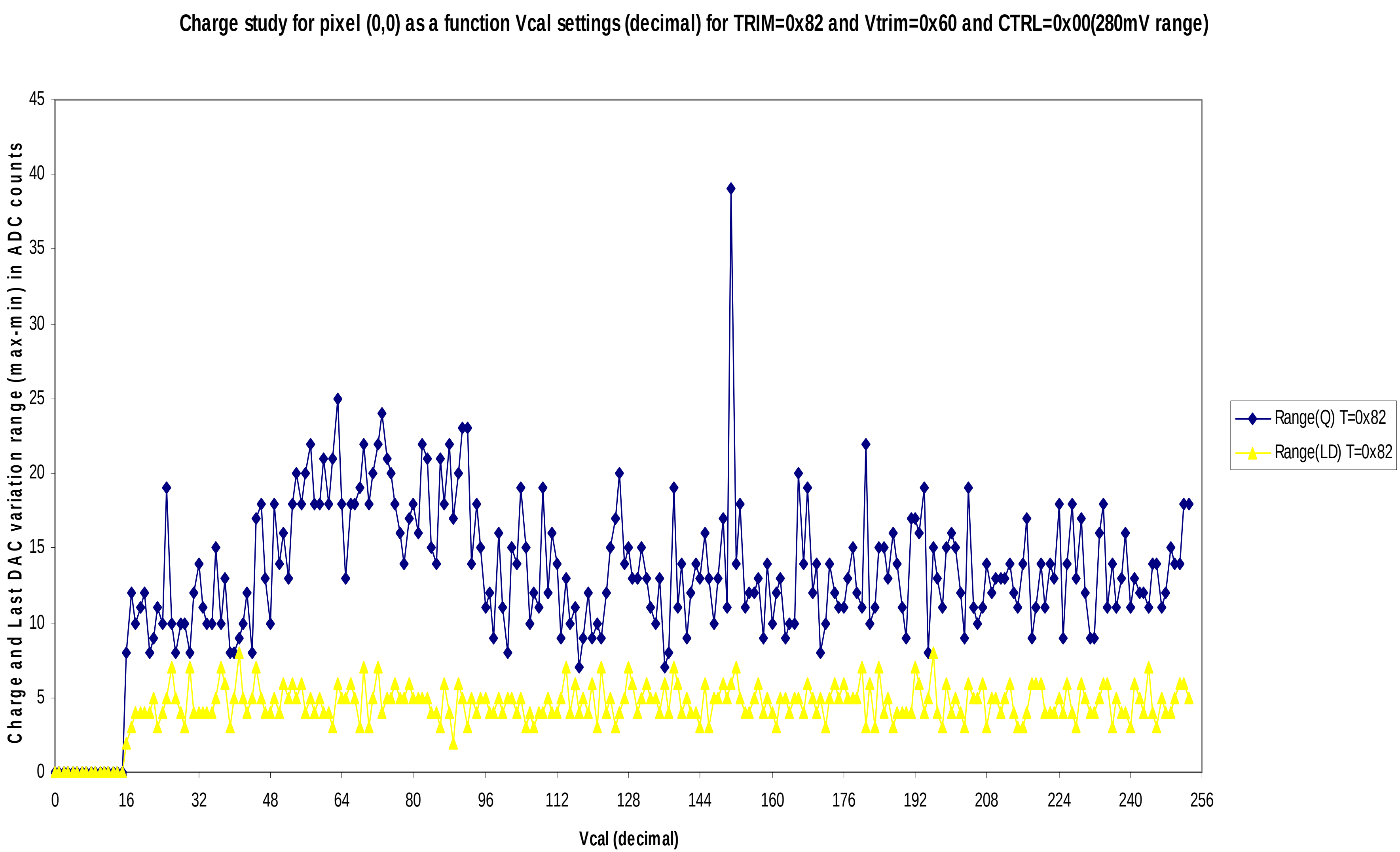
Pixel's charge dependence



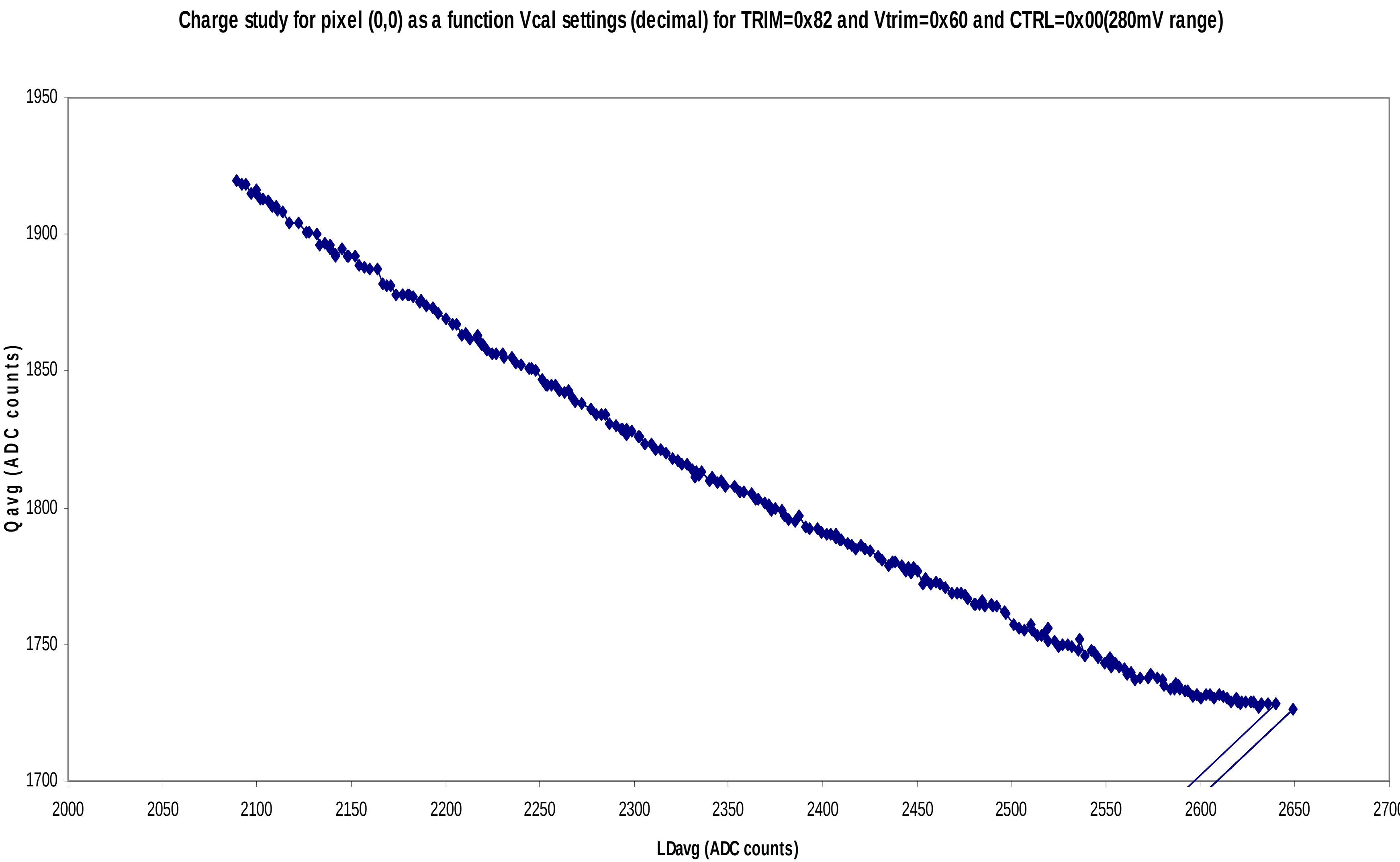
Pixel's charge dependence



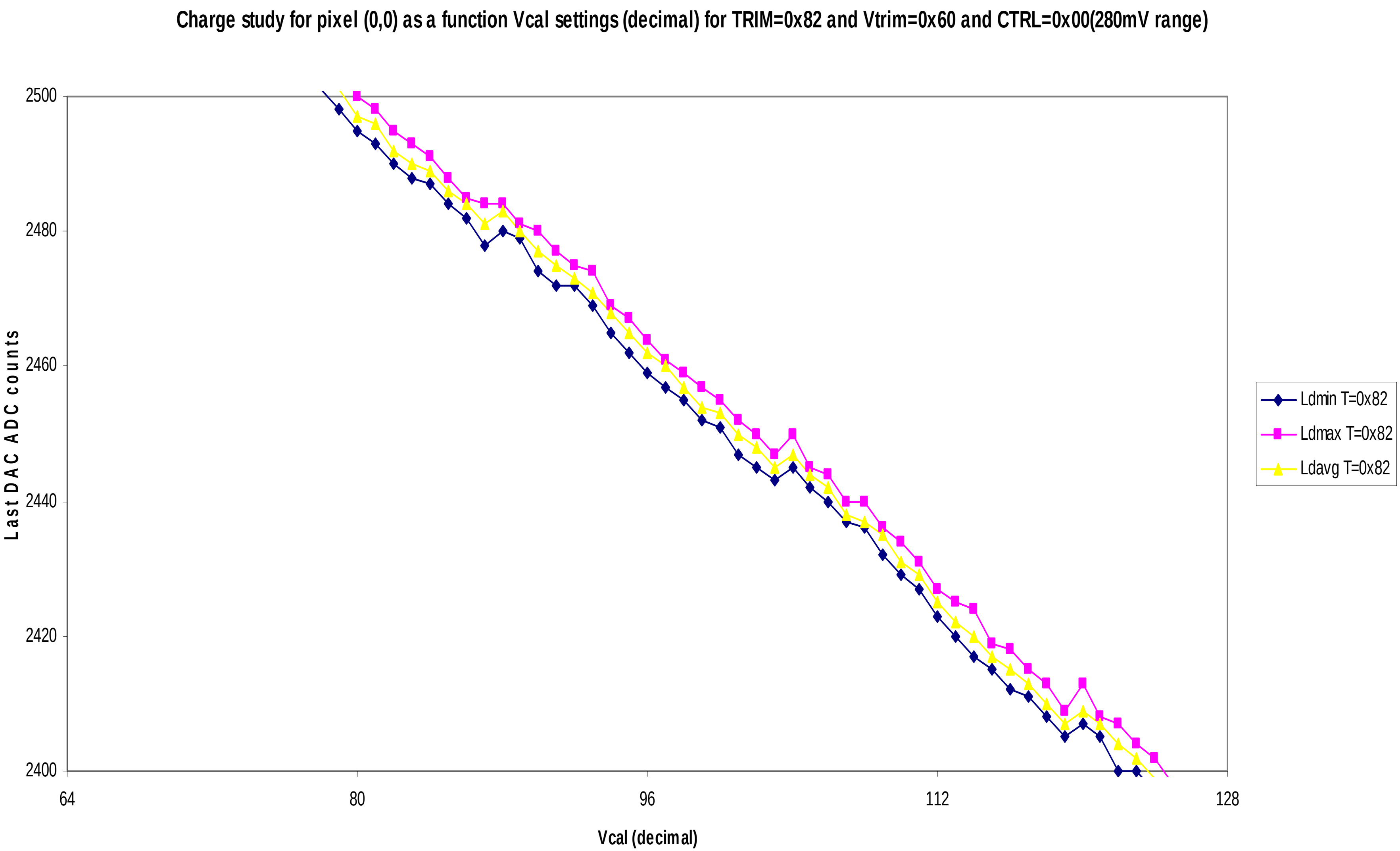
Pixel's charge dependence



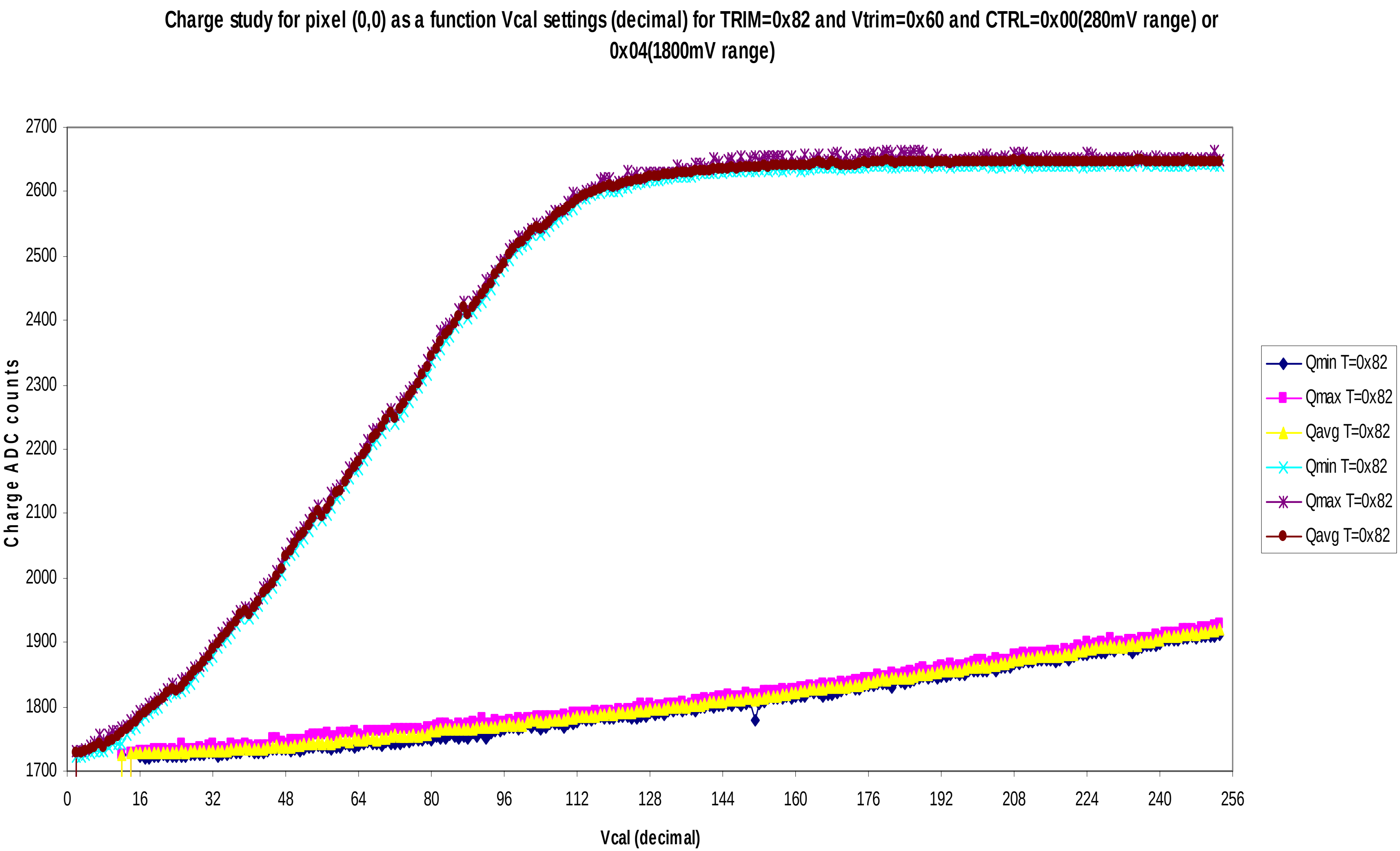
Pixel's charge dependence



Pixel's charge dependence

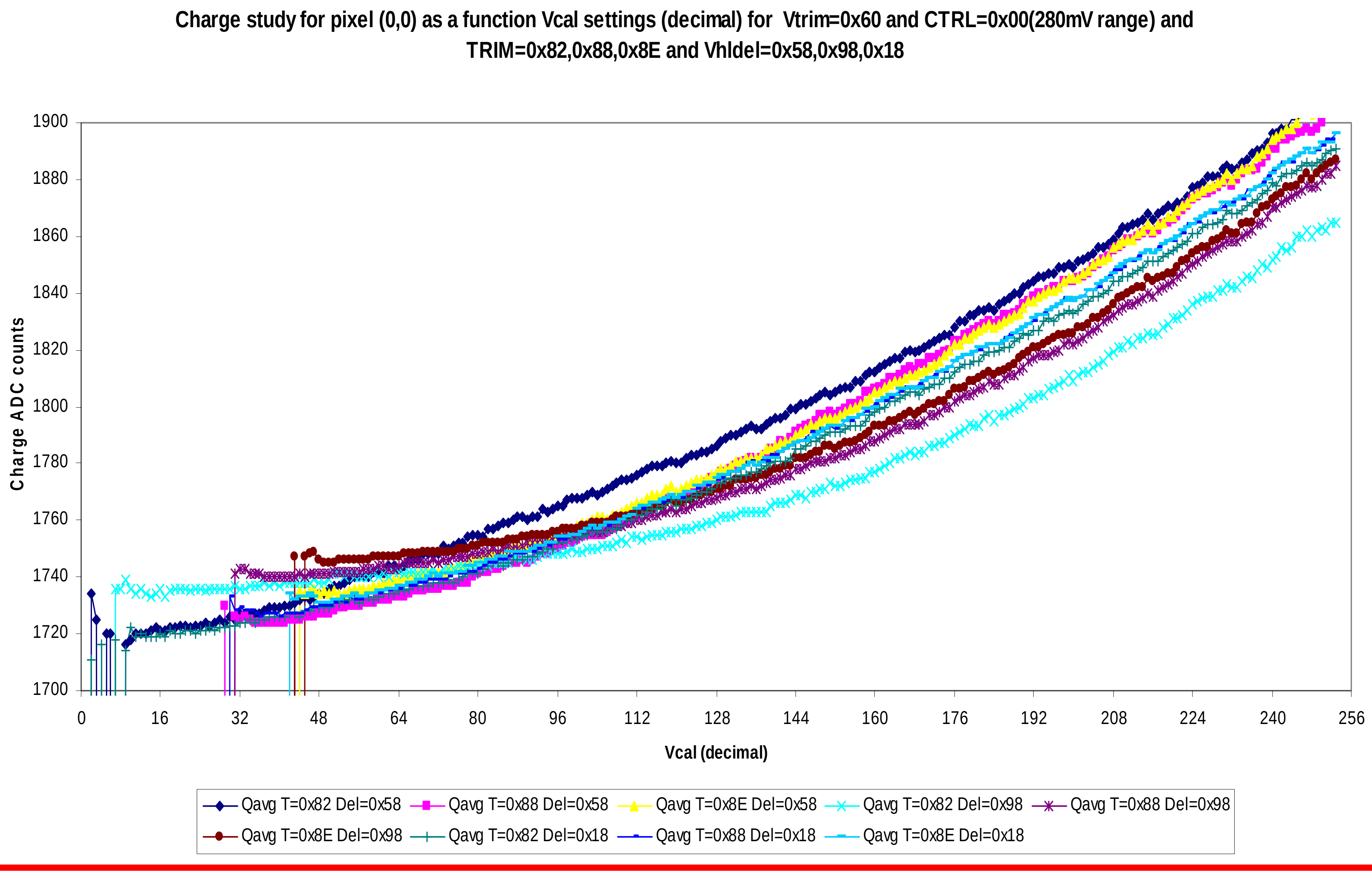


Pixel's charge dependence



Pixel's charge dependence

Pixel's charge dependence



Multiple hit problem (followup)

- The multiple hit problem (mentioned earlier in slide 4) was my big problem in proceeding with wafer testing. In fact the effort to eliminate it generated most of the above investigations!
- One of the first 'improvement' in eliminating the multiple hits was the following: before staring the chip test, when programming all pixels with mask and trim bits (there is not a power-on defined state), instead of enabling all pixels and set their trim bits to 0x88 as I did for V1 and PSI43 chip, I followed Roland's setup, in which all pixels are configured disabled and trim bits are also disabled (0x0F). Although this approach is not right (in my opinion) it seems to be very helpful in avoiding multiple hit problem. But again, this is not the way the chip is operated (with all pixels killed and only the one which is tested being enabled and calibrated).
- Now, after about two weeks of periodic phone discussions we found another difference in our testing procedures, which might not seems to be very important on a first look. It is the WBC register setting (write bunch cross number register). I used so far a value of 27decimal. Roland is using a value of 130decimal. With WBC=27 I have plenty of multiple hits if all pixels are enabled and just one calibrated, and no multiple hits at all if all pixels are disabled and just one enabled and calibrated. With WBC=130 I have no multiple hits regardless the enable/disable state of all the others pixels. This might be due to more clock cycles that are needed by V2 to 'process' the information (compared with V1). This explanation is agreed by Roland too, although at this moment is not completely understood. I didn't investigate what is the minimum WBC number for which the chip is not giving multiple hits (might be just a few numbers up from 27!). So, from now on I'll use WBC=130.

Assigning error codes for each pixel

```
********************************************************
REPORTING ANALOG LEVELS HISTOGRAM
more then six analog clusters found for column/row address
more then one analog cluster found for charge Q
********************************************************
```

	BIN(min)	BIN(max)	ADDRESS	CHARGE
1	0	15	0	0
2	16	31	0	0
3	32	47	0	0
4	48	63	0	0
5	64	79	0	0
6	80	95	0	0
7	96	111	0	0
…………………				
115	1824	1839	0	5
116	1840	1855	0	31
117	1856	1871	0	139
118	1872	1887	0	303
119	1888	1903	1587	575
120	1904	1919	1027	830
121	1920	1935	708	1118
122	1936	1951	3080	1392
123	1952	1967	3124	1593
124	1968	1983	1331	1509
125	1984	1999	471	1319
126	2000	2015	546	1184
127	2016	2031	0	872
128	2032	2047	0	639
129	2048	2063	0	309
130	2064	2079	1770	146
131	2080	2095	1671	31
132	2096	2111	457	2
133	2112	2127	2579	0
134	2128	2143	3306	0
135	2144	2159	1643	0
136	2160	2175	623	0
137	2176	2191	125	0
138	2192	2207	0	0
139	2208	2223	0	0

- Since there are more measurements for each pixel, I need to keep track of each measurement's pass or fail result. There are a total of nCol*nRow*nMaskTrim possible failures in the pixels' area, where nCol=52, nRow=80 are the number of columns and rows and nMaskTrim is the number of trim settings exercised for each pixel response test (for example if we do measure pixel response for trim bits 0x84, 0x88 and 0x8C then nMaskTrim=3)
- Each of the above measurements, if failed, receives an error code:
  - C1,C2… if column not found in the test data
  - F1,F2… if there is a system FIFO error when scanning Vcal
  - N1,N2… if the pixel does not respond to any Vcal in the investigated range
  - M1,M2… if the pixel does not responded with exactly one hit or exactly no hit (I call it multiple hits or partial hits) when scanning Vcal
  - FD1,FD2… if there is a system FIFO error when pixel was disabled
  - D1,D2… if the pixel does respond when disabled (unable to disable)
- The next step is constructing an analog level histogram for addresses and another analog level histogram for charge readouts, over all pixels. The histograms' bin width can be changed (in the left example it is 16 counts). Based on these histograms, min and max for each of the six analog levels for addresses and respectively min and max for the charge variation are determined (see next slide).
- Once we know the variation range for each of the six analog levels, the next step is to find pixels with wrong analog level responses and give them a new error code:
  - L1C0,L2C0…L1A2,L2A2… if wrong level for C0,C1,A0,A1 or A2

Reporting statistic on column, row and charge levels

```
*********************************************
          LEV(min)    LEV(max)  RANGE   GAP
*********************************************
L0        1903        2032      129
L2        2063        2176      113     31
L3        2223        2336      113     47
L4        2367        2496      129     31
L5        2527        2640      113     31
L6        2671        2784      113     31
Q         1663        1920      257
*********************************************
PARAM   AVERAGE   MIN     MAX     ENTRIES
*********************************************
TVS       1.88    0       4       4160
TVI      92.58    64      128     4160
TVR2      0.79    0       1       4160
PED      2082     2080    2085    4160
UBK      1508     1506    1511    4160
BK       2022     2020    2025    4160
Q        1792     1675    1896    4160
CLev1    1970     1920    1999    1760
RLev1    1966     1918    2018    2288
CLev2    2126     2075    2154    1760
RLev2    2119     2073    2172    2392
CLev3    2279     2229    2296    1600
RLev3    2273     2227    2326    2418
CLev4    2433     2384    2451    1600
RLev4    2424     2381    2479    2262
CLev5    2576     2536    2602    960
RLev5    2574     2533    2630    1794
CLev6    2708     2680    2737    640
RLev6    2716     2676    2772    1326
*********************************************
```

- The min, max and range of each analog levels L0,L1…L6 together with the gap between levels are reported (see left report, top part).
- Now that we know where the analog levels are for this chip, the next step is to do a statistic on all measurements done on a single pixel, thus providing some 'final' parameters for each pixel: the average values for pedestal, ultra black, black, C0, C1, A0, A1, A2 and charge. I also compute the slope, intercept and correlation for a linear best-fit of the Vcal (at which pixel fires) versus trim bits setting. This statistic calculations are done over all measurements of one pixel, if all of them have no error flags. If at least one measurement fails, that pixel is not assigned any statistic parameters and the first error code found is assigned as an error flag for that pixel.
- Since we have now unique parameter values for each pixel (regardless how many time and in what conditions it was measured) the next obvious step is to do a statistic of same parameters over all 4160 pixels (of course the failed pixel will not be included). The result are reported in the bottom part of the left example.
- We are now close to an end of our pixel failure analysis, but we need a sort of summary of all the above to help us having a picture of what was wrong with each pixel and somehow decide if this is a good die or not. The final decision is not yet implemented in software, because of the luck of criteria at this time. But we do have the following to help us – see next slide.

```
*****************************************************************************
REPORTING DEFECTIVE PIXELS ON EACH COLUMN
*****************************************************************************
COL25 found 1 defective pixels:ROW42L2A0,
COL27 found 80 defective pixels:ROW1N1,N2,N3,ROW2N1,N2,N3,ROW3N1,N2,N3,ROW4N1,N2,N3,ROW5N1,N2,N3,
COL28 found 80 defective pixels:ROW1N1,N2,N3,ROW2N1,N2,N3,ROW3N1,N2,N3,ROW4N1,N2,N3,ROW5N1,N2,N3,
COL35 found 1 defective pixels:ROW7L2A0,
COL36 found 3 defective pixels:ROW61L3A0,ROW75L1A0,ROW77L3A0,
COL42 found 1 defective pixels:ROW75N1,N2,N3,
*****************************************************************************
```

Reporting defective pixels

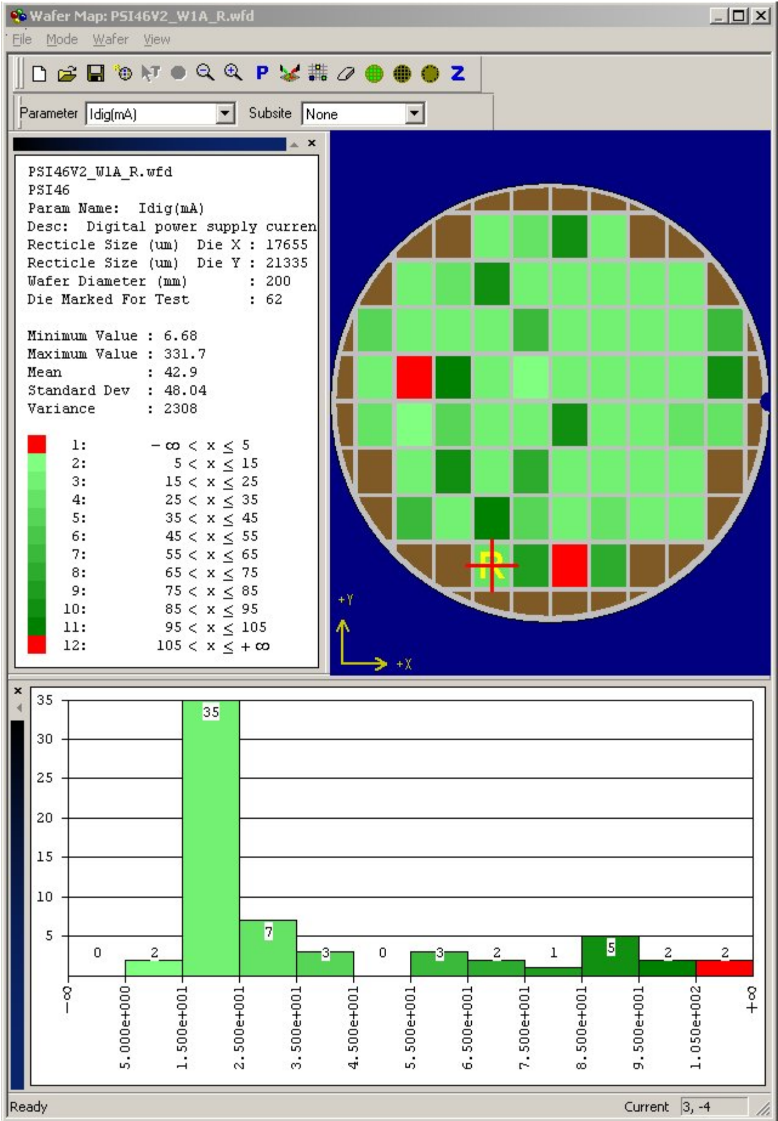
```
****************************************************************************
REPORTING DEFECTIVE PIXELS ON EACH COLUMN
****************************************************************************
COL25 found 1 defective pixels:ROW42L2A0,
COL27 found 80 defective pixels:ROW1N1,N2,N3,ROW2N1,N2,N3,ROW3N1,N2,N3,ROW4N1,N2,N3,ROW5N1,N2,N3,ROW6N1,N2,N3,ROW7N1
COL28 found 80 defective pixels:ROW1N1,N2,N3,ROW2N1,N2,N3,ROW3N1,N2,N3,ROW4N1,N2,N3,ROW5N1,N2,N3,ROW6N1,N2,N3,ROW7N1
COL35 found 1 defective pixels:ROW7L2A0,
COL36 found 3 defective pixels:ROW61L3A0,ROW75L1A0,ROW77L3A0,
COL42 found 1 defective pixels:ROW75N1,N2,N3,
****************************************************************************
```

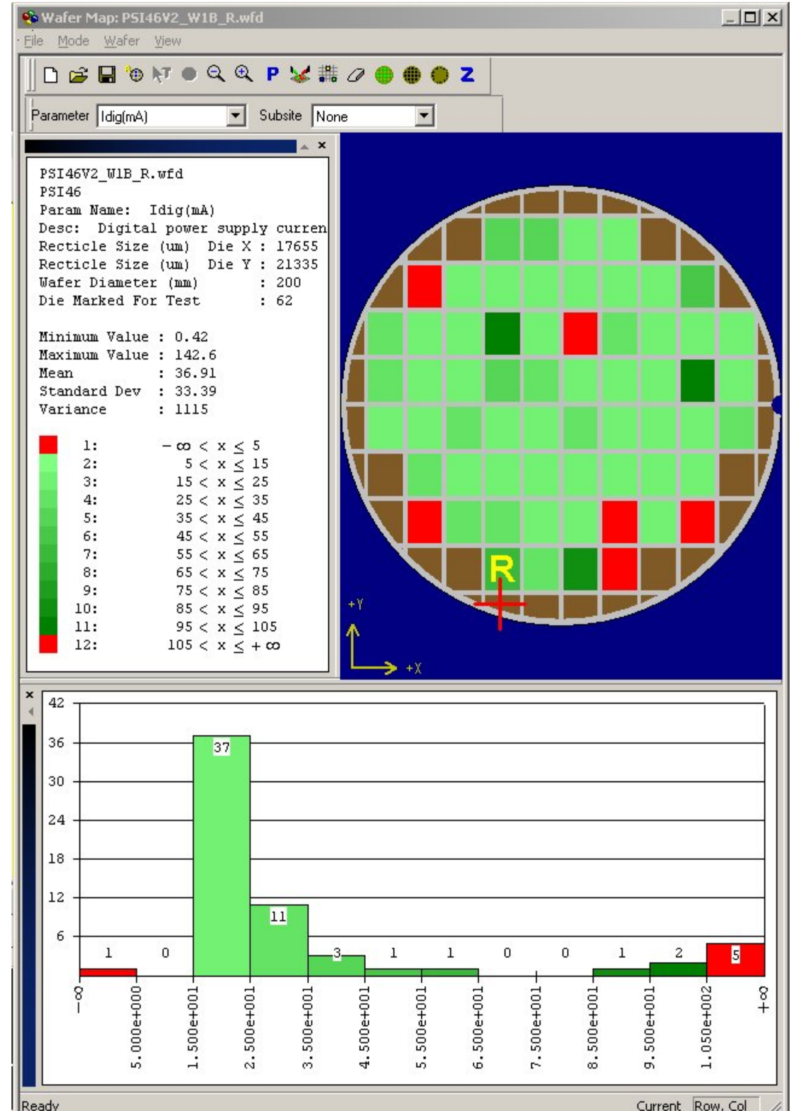
```
*****************************************************
TOTAL NUMBER OF DEFECTIVE PIXELS = 166 from 4160
*****************************************************
    0000000001111111111222222222233333333334444444444555
    1234567890123456789012345678901234567890123456789012
80  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
79  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
78  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
77  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOXOOOOOOOOOOOOOOOO
76  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
75  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOXOOOOOXOOOOOOOOOO
74  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
73  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
72  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
71  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
70  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
69  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
68  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
67  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
66  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
65  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
64  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
63  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
62  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
61  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOXOOOOOOOOOOOOOOOO
60  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
59  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
58  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
57  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
56  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
55  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
54  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
53  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
52  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
51  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
50  OOOOOOOOOOOOOOOOOOOOOOOOOOXXOOOOOOOOOOOOOOOOOOOOOOOO
```

- This is a report of defective pixels in each column (see above). It gives us the total number of defective pixels and, for the curious guys, the pixel row number and the test on which it failed. For example, in column 36 we have three defective pixels, in rows 61, 75 and 77. All three pixels failed because of wrong level address for the analog bit A0. Note that pixels (25,42) and (35,7) have the same failure type, while pixel (42,75) and all pixels in columns 27 and 28 are not responding.
- There is also a map with 80 rows and 52 columns (see left). A "O" marks a good pixel, while an "X" is a defective one.

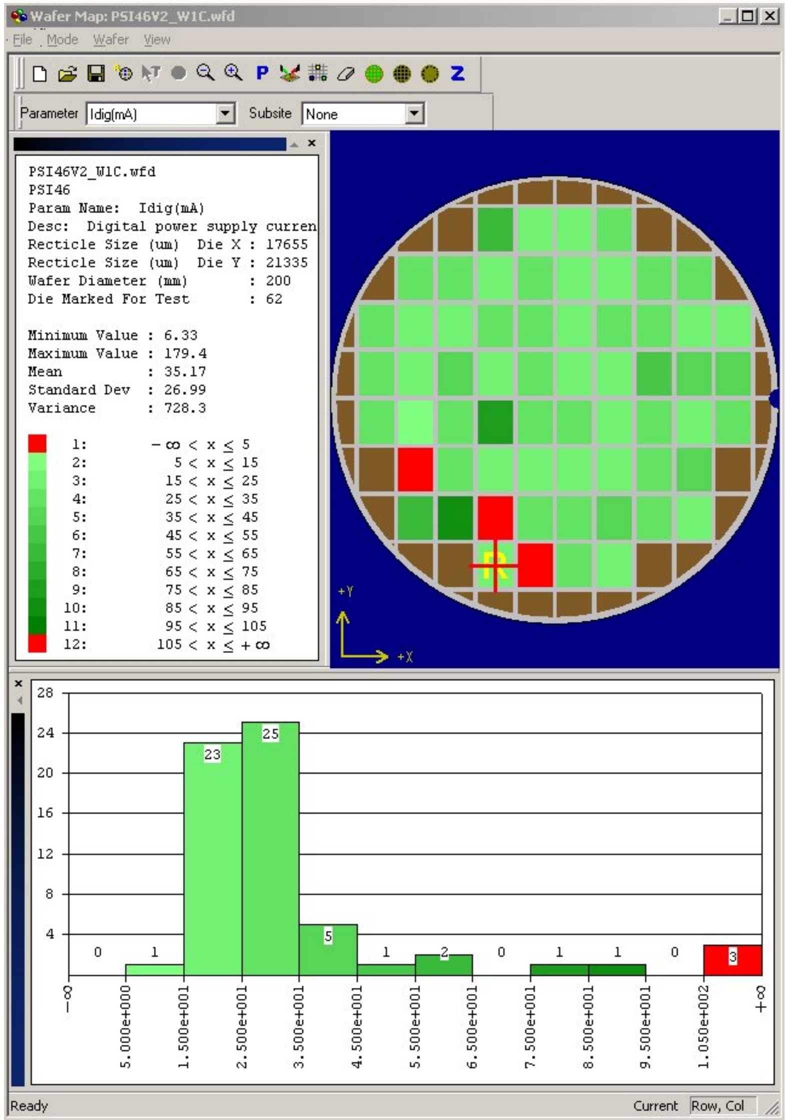
IMPORTANT NOTE: Although the analog levels can be, in general, separated in exactly six classes, the variation from die to die does not allow us to use the same limits on a wafer, or the yield will be dramatically lowered. This might be explained by the larger nonlinearity observed for DAC registers that control the analog levels (see slide 3). If we accept this approach also in the production, then we need to 'align' these levels for different chips by programming different values in the chip readout registers VIbias_PH, VIbias_ROC, VIbias_DAC.

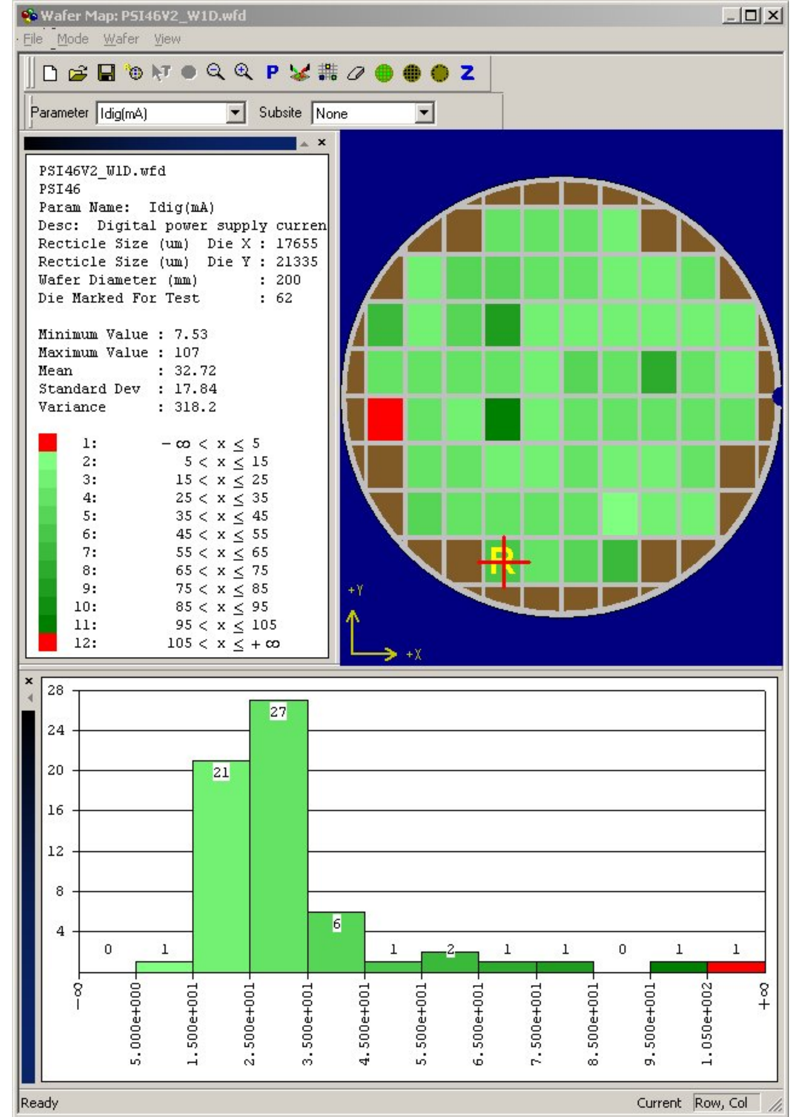
Wafer K7MWH6T test results (Idig A and B chips)



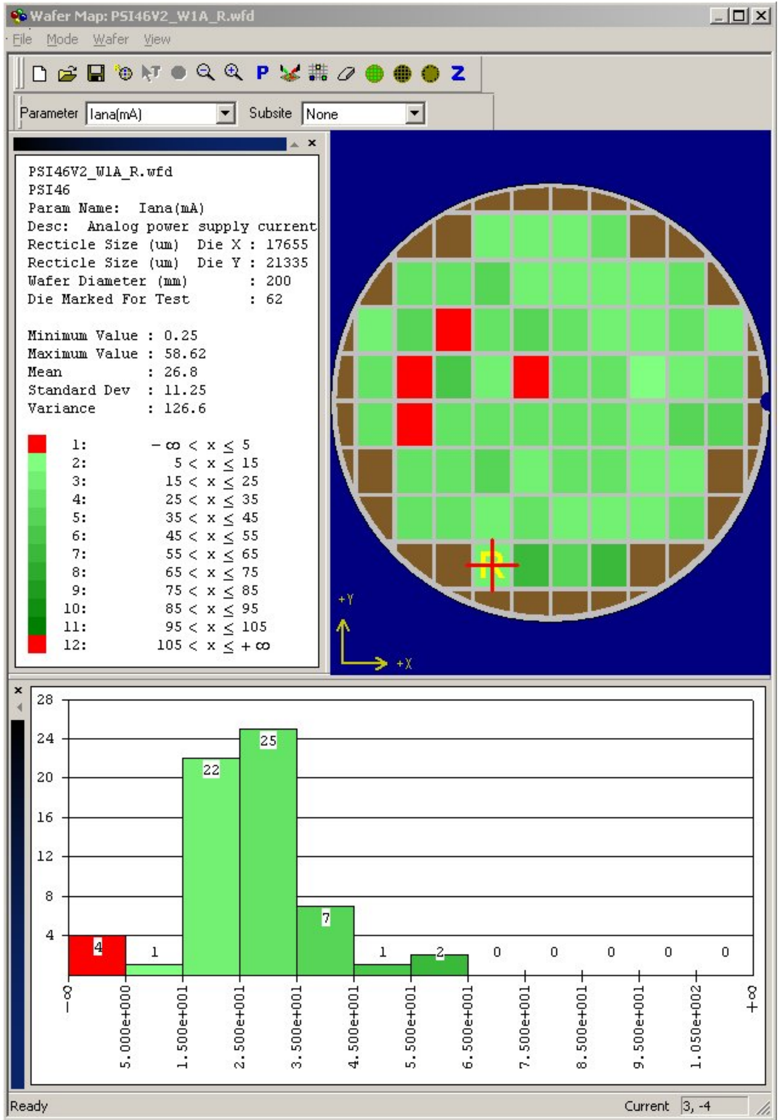


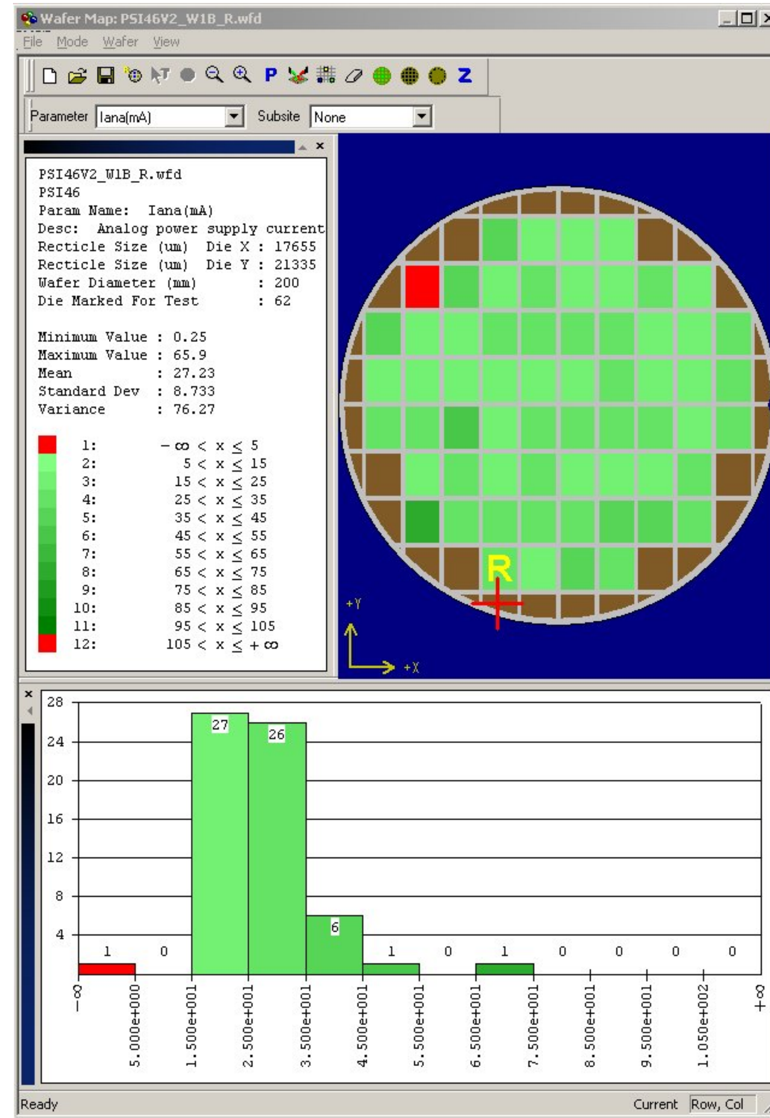
Wafer K7MWH6T test results (Idig C and D chips)



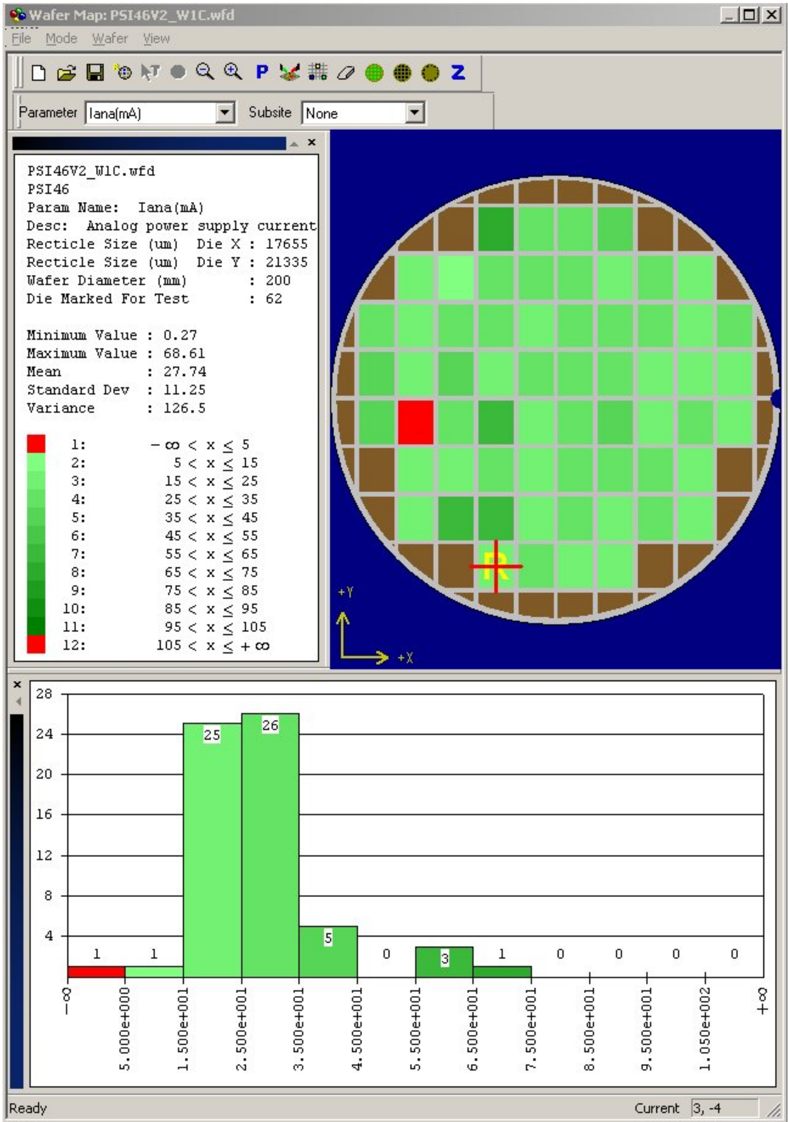


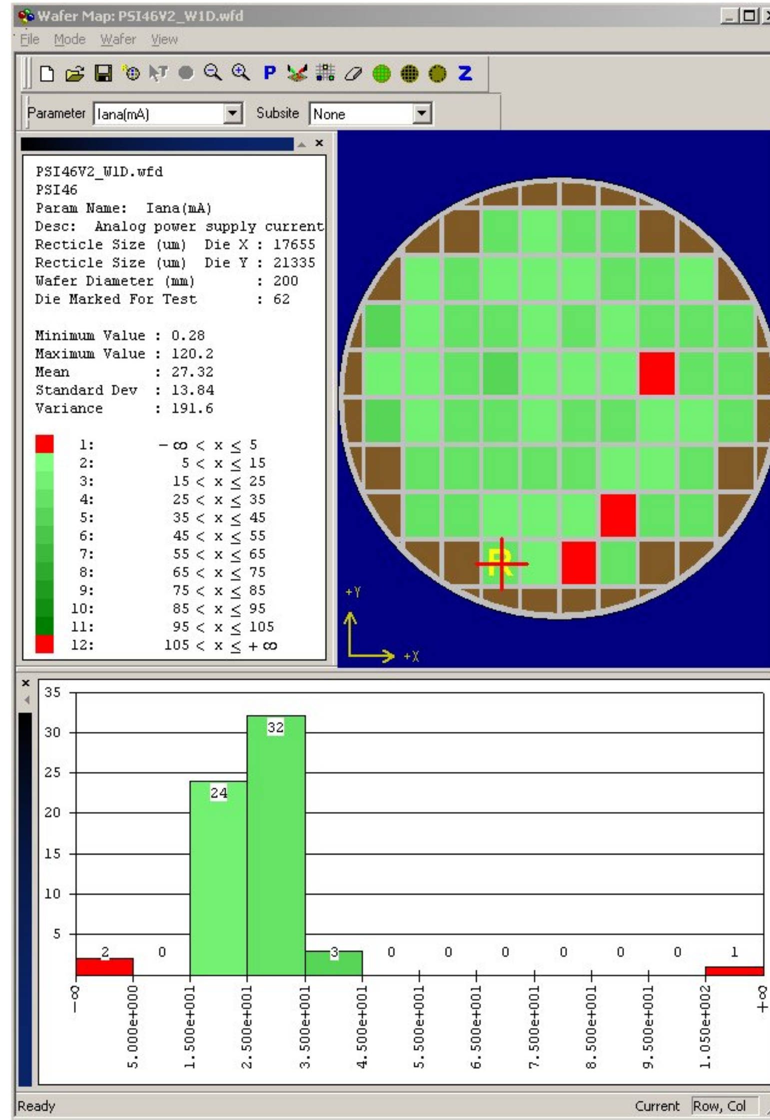
Wafer K7MWH6T test results (Iana A and B chips)



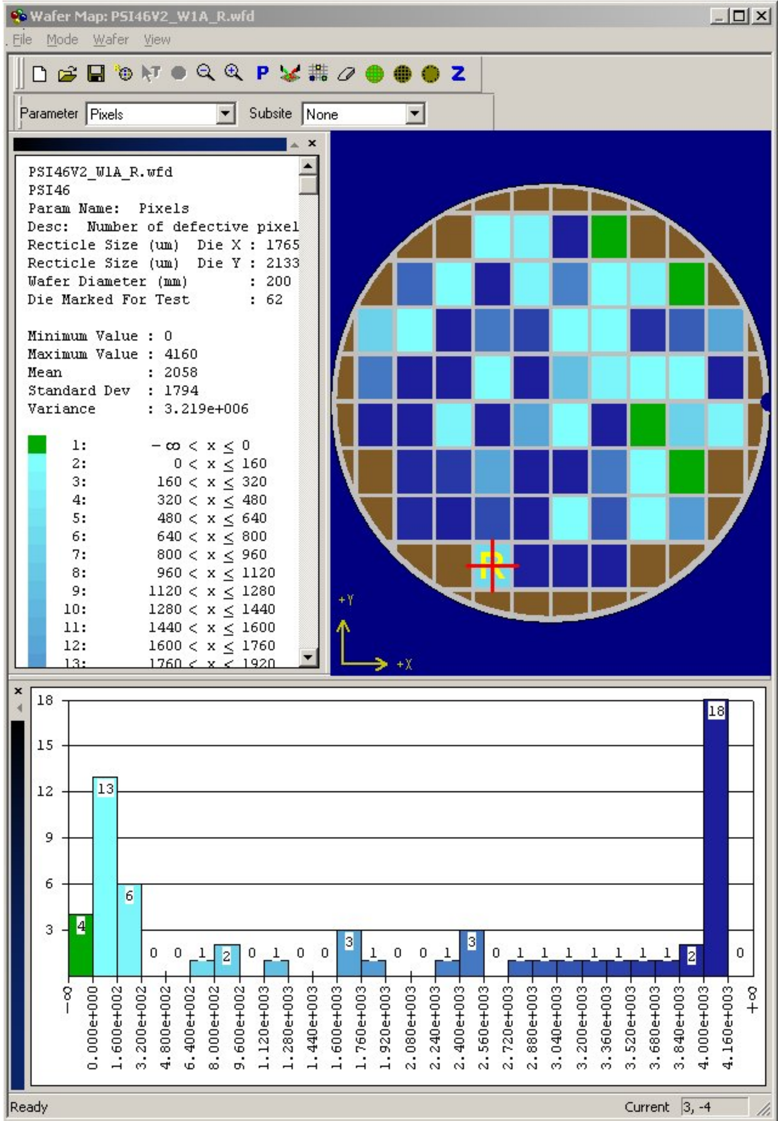


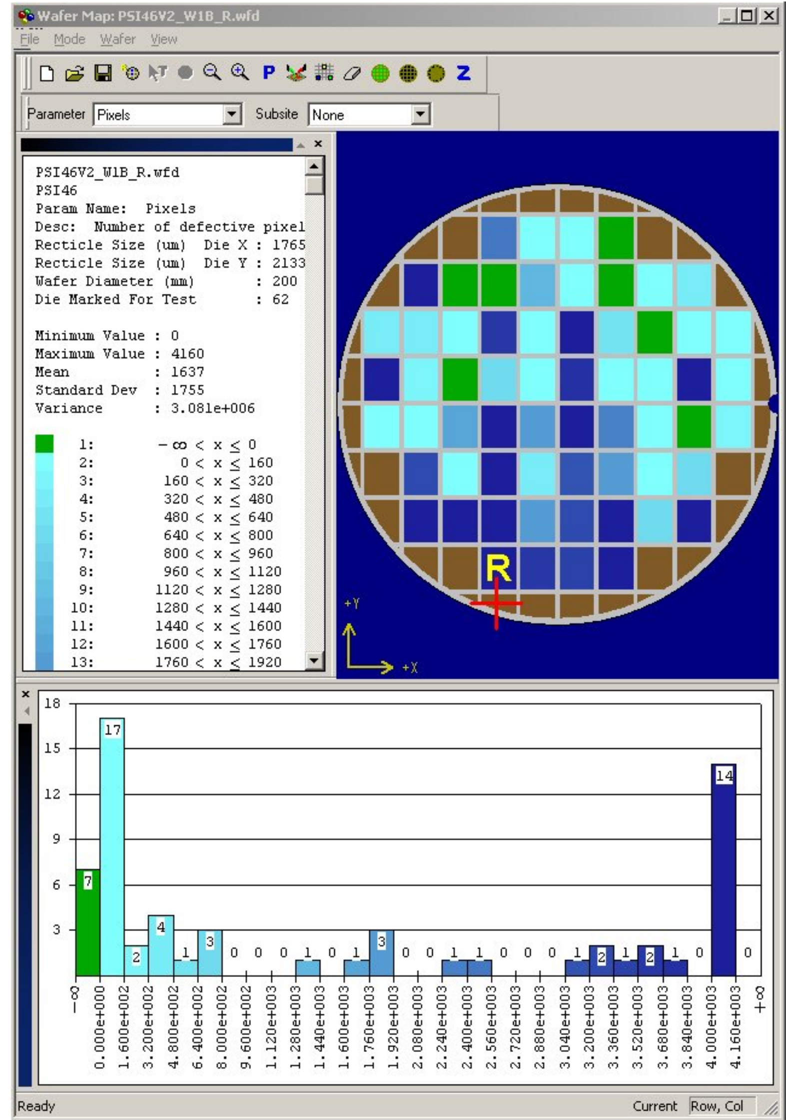
Wafer K7MWH6T test results (Iana C and D chips)



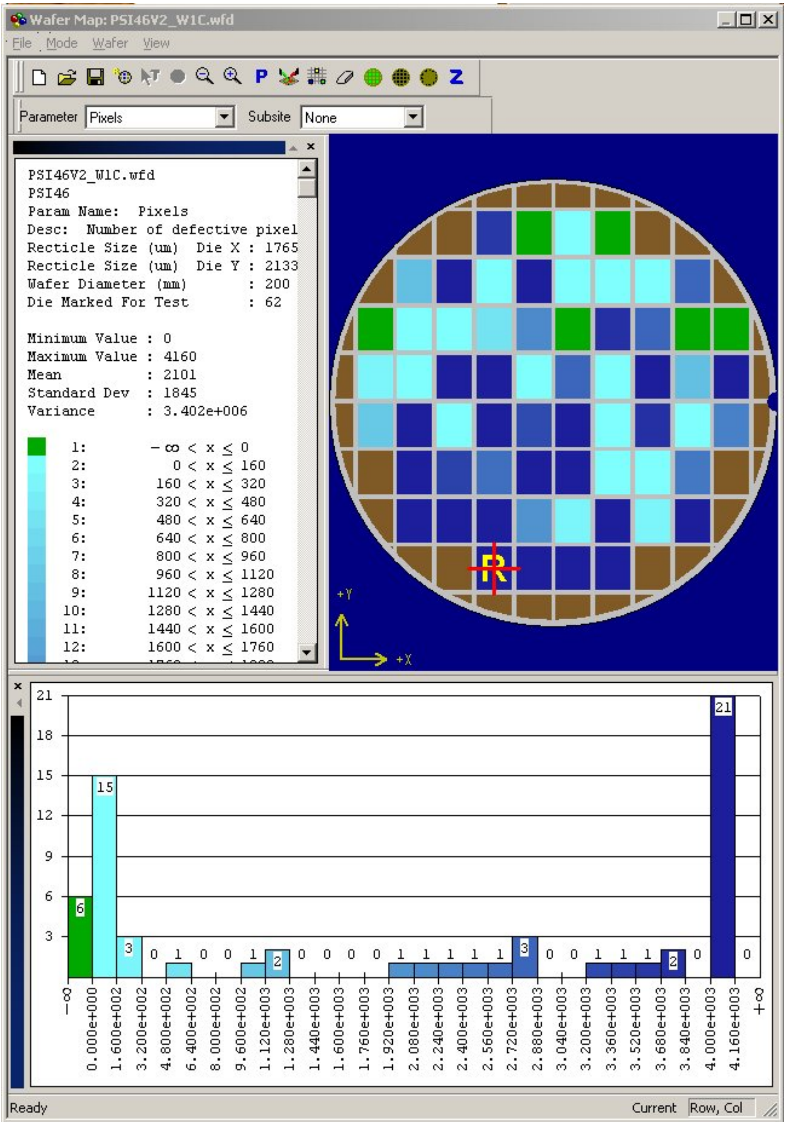


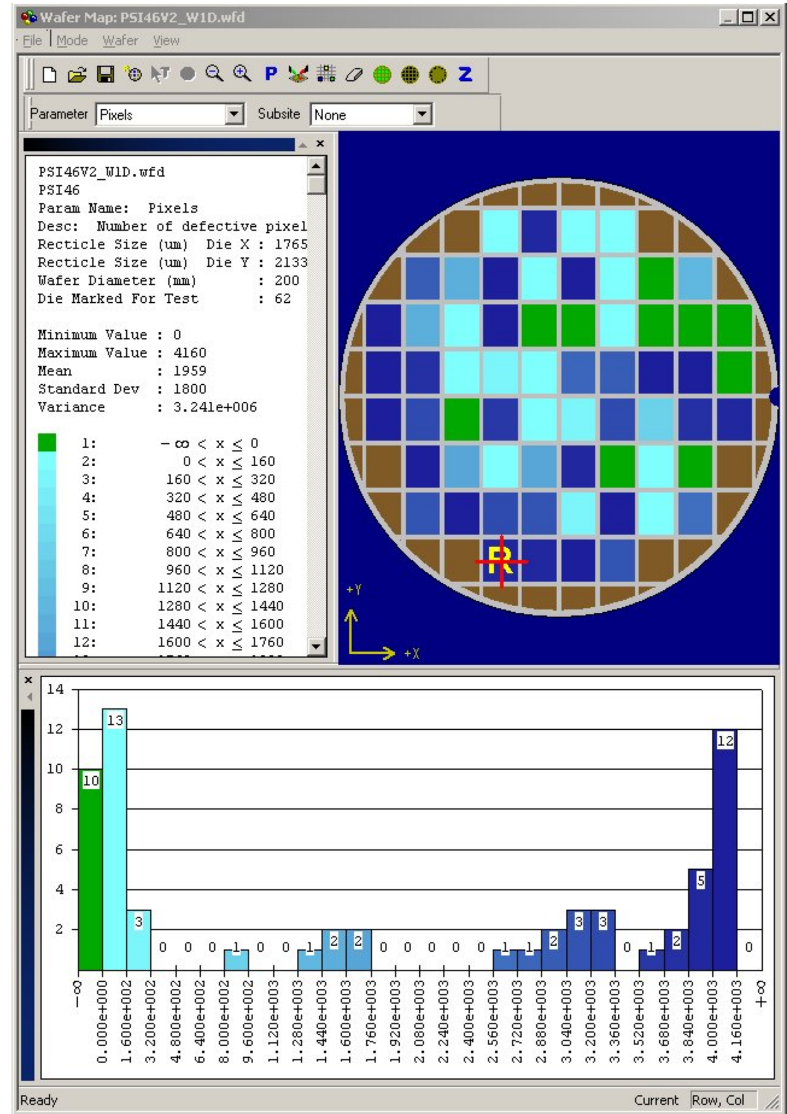
Wafer K7MWH6T test results (dfct.pix. A and B chips)





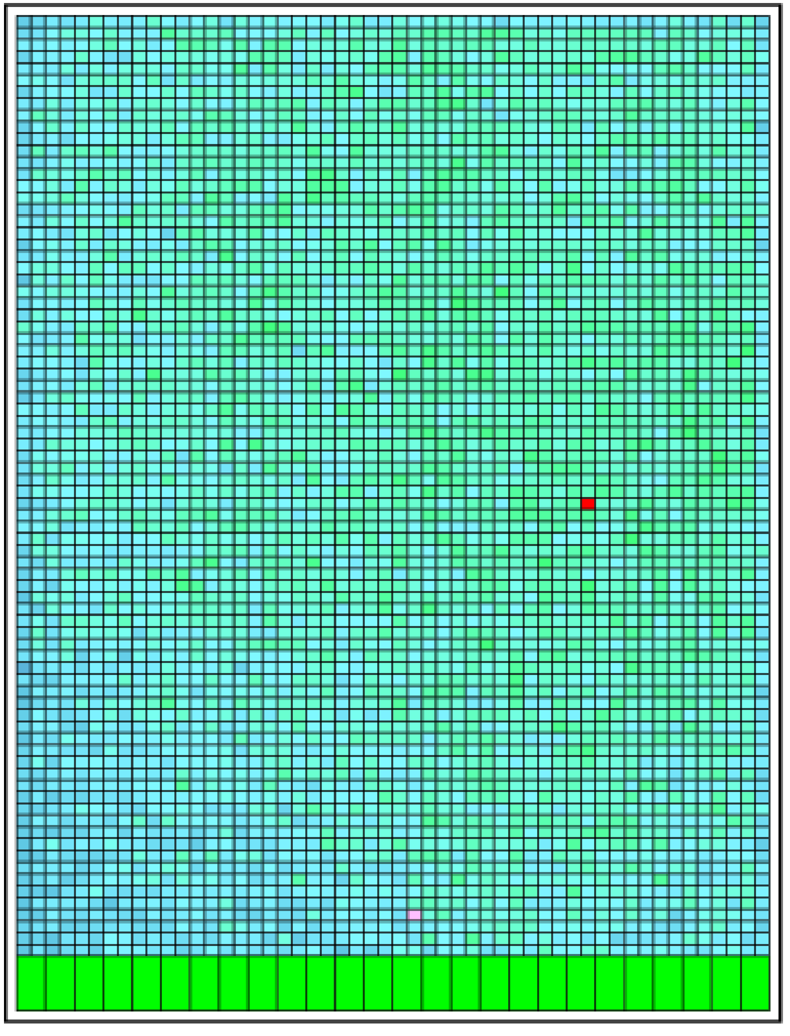
Wafer K7MWH6T test results (dfct.pix. C and D chips)





Wafer K7MWH6T - PSI vs. FNAL test results

PSI46V2 K7MWH6T/1 03A

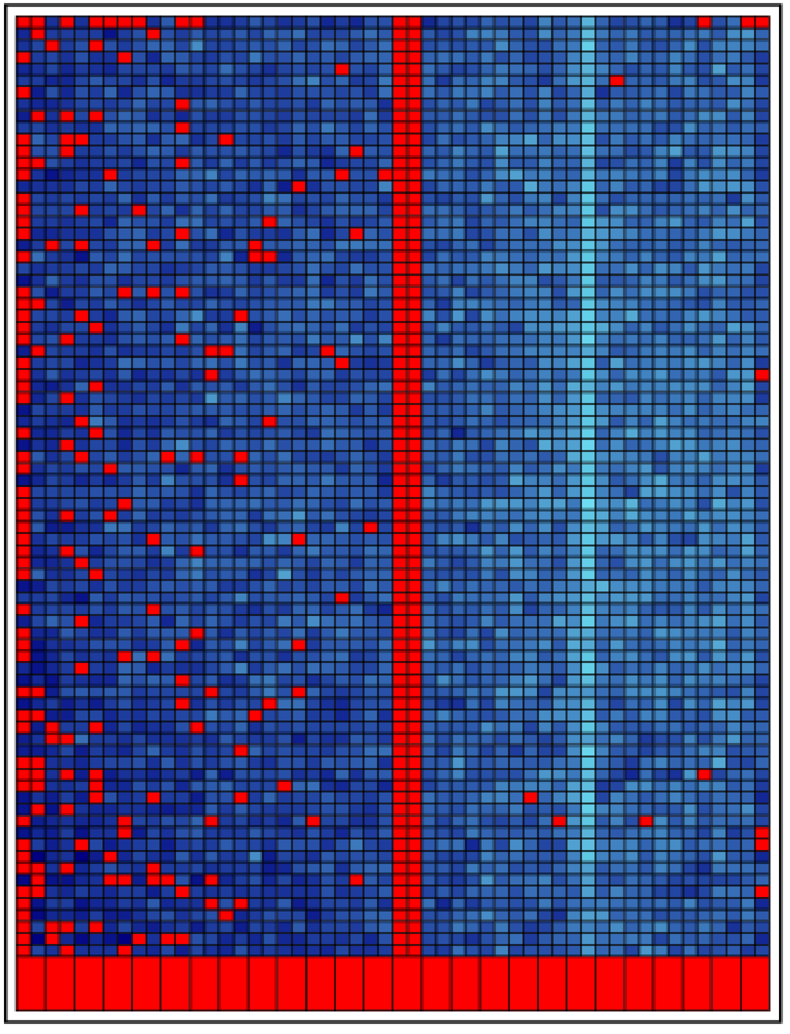


- This is chip A59 for us.
- PSI wafer map report say 1 pixel defect

```
*************************************************************
REPORTING DEFECTIVE PIXELS ON EACH COLUMN
*************************************************************
COL40 found 1 defective pixels:ROW39N1,N2,N3,
*************************************************************
TOTAL NUMBER OF DEFECTIVE PIXELS = 1 from 4160
*************************************************************
```

Wafer K7MWH6T PSI vs. FNAL test results

PSI46V2 K7MWH6T/1 04A



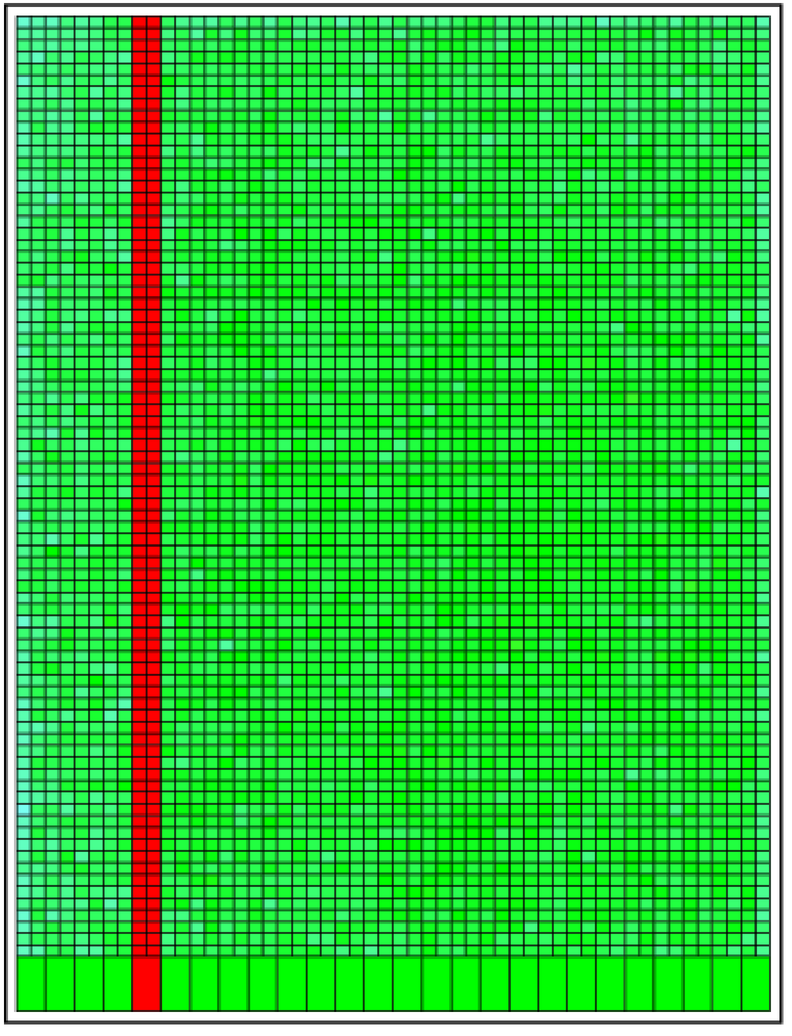
- This is chip A60 for us.
- PSI wafer map report say >=5 dcol defect (?)

```
**********************************************************
REPORTING DEFECTIVE PIXELS ON EACH COLUMN
**********************************************************
COL25 found 1 defective pixels:ROW42L2A0,
COL27 found 80 defective pixels:ROW1N1,N2,N3,ROW2N1,N2,N
COL28 found 80 defective pixels:ROW1N1,N2,N3,ROW2N1,N2,N
COL35 found 1 defective pixels:ROW7L2A0,
COL36 found 3 defective pixels:ROW61L3A0,ROW75L1A0,ROW77
COL42 found 1 defective pixels:ROW75N1,N2,N3,
**********************************************************
TOTAL NUMBER OF DEFECTIVE PIXELS = 166 from 4160
**********************************************************
```

- Then, chip A61 is a short in both PSI and FNAL report (we measured Idig=94mA)
- Then, chip A62 is PERFECT in both reports
- Then, chip A58 is PERFECT in both reports

Wafer K7MWH6T PSI vs. FNAL test results

PSI46V2 K7MWH6T/1 17A

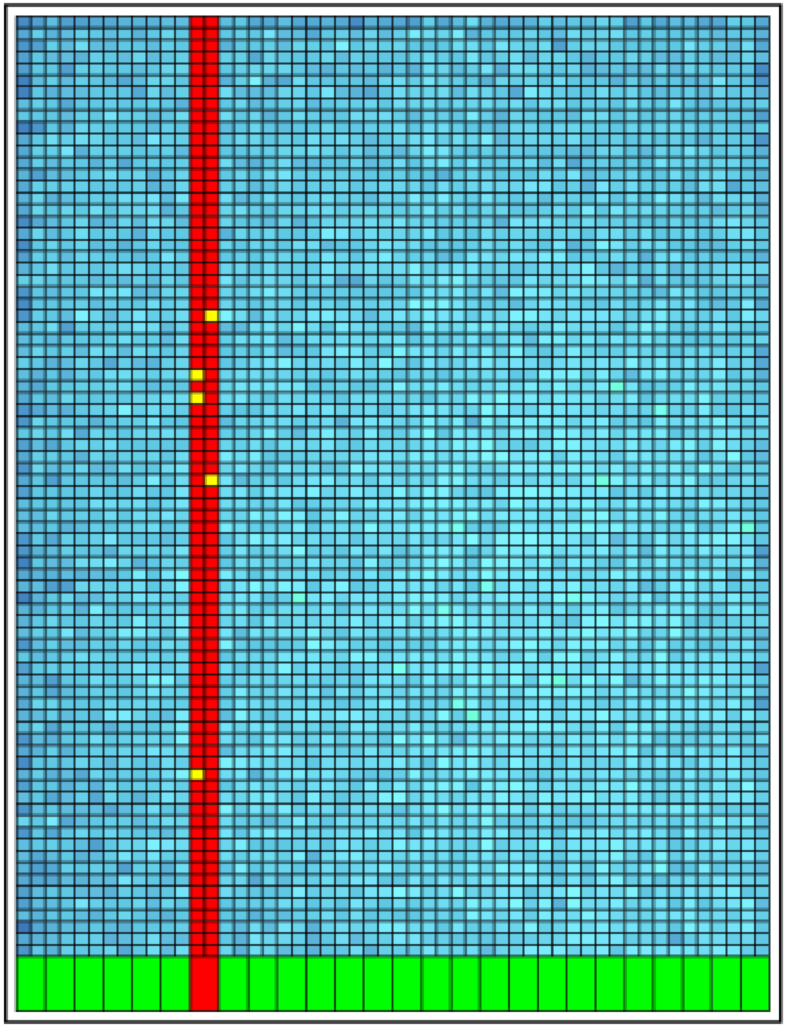


- This is chip A57 for us.
- PSI wafer map report say 1 dcol defect
- FNAL found an additional pixel defect

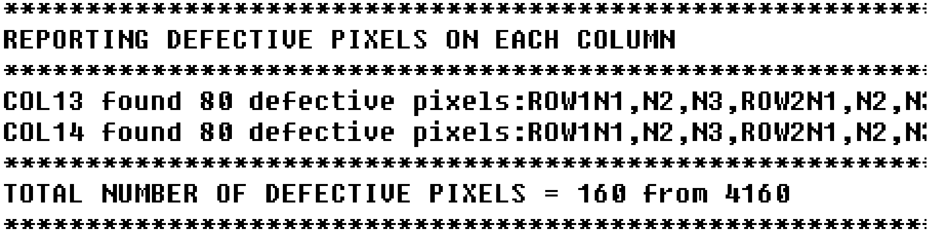
```
********************************************************
REPORTING DEFECTIVE PIXELS ON EACH COLUMN
********************************************************
COL2 found 1 defective pixels:ROW73N1,N2,N3,
COL9 found 80 defective pixels:ROW1N1,N2,N3,ROW2N1,N2,N3
COL10 found 80 defective pixels:ROW1N1,N2,N3,ROW2N1,N2,N:
********************************************************
TOTAL NUMBER OF DEFECTIVE PIXELS = 161 from 4160
********************************************************
```

Wafer K7MWH6T PSI vs. FNAL test results

PSI46V2 K7MWH6T/1 16A

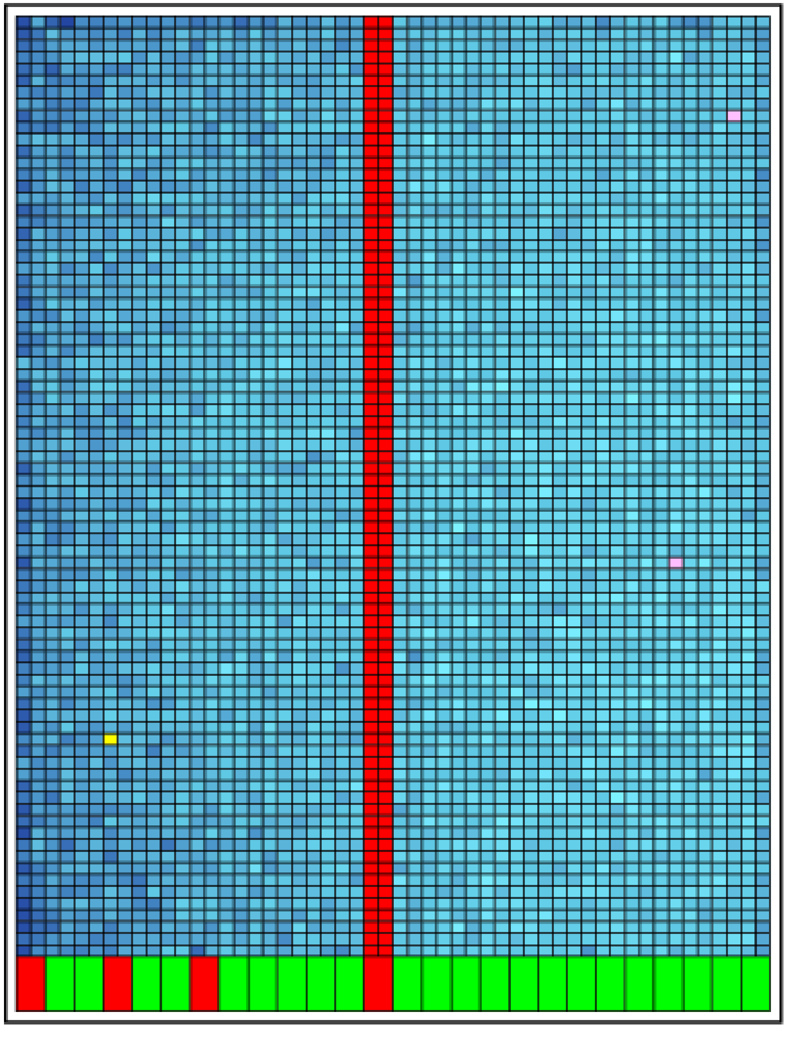


- This is chip A56 for us.
- PSI wafer map report say 1 dcol defect



Wafer K7MWH6T PSI vs. FNAL test results

PSI46V2 K7MWH6T/1 15A



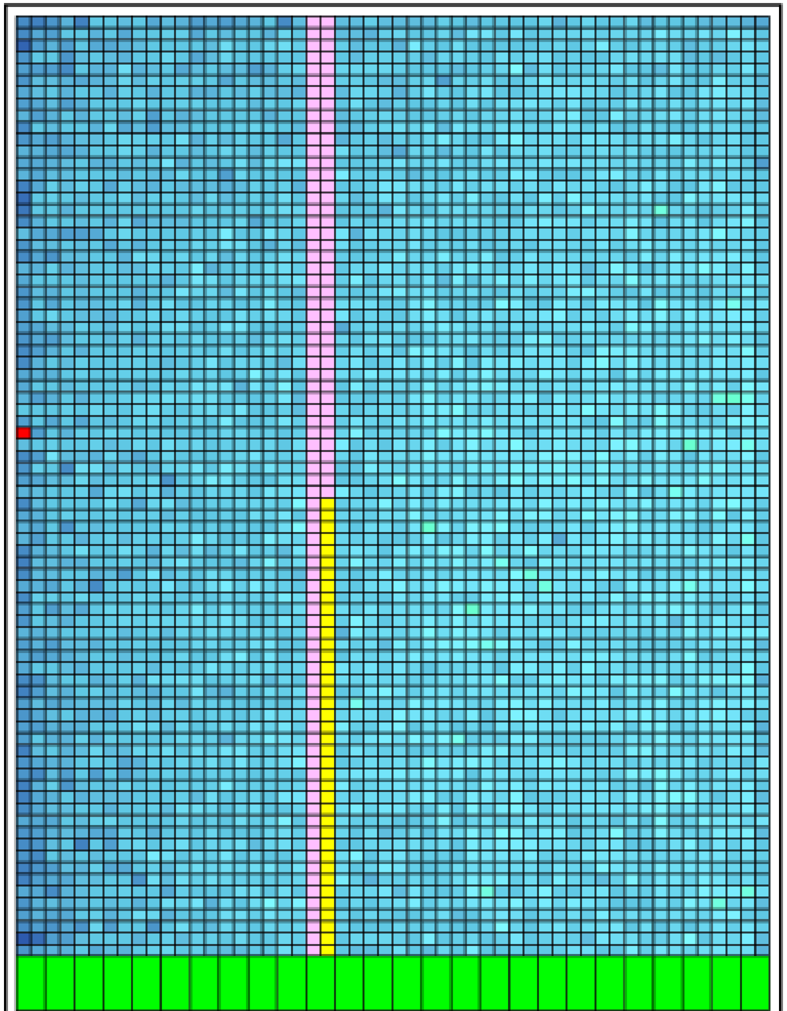
- This is chip A55 for us.
- PSI wafer map report say 2…4 dcol defect (?)
- FNAL one test shows oscillations from COL27 up
- FNAL second test shows two more pixels defective
- The agreement between tests is questionable here

```
*************************************************************
REPORTING DEFECTIVE PIXELS ON EACH COLUMN
*************************************************************
COL7 found 80 defective pixels:ROW1N1,N2,N3,ROW2N1,N2,N3
COL8 found 80 defective pixels:ROW1N1,N2,N3,ROW2N1,N2,N3
COL26 found 31 defective pixels:ROW50N1,D1042,F2,FD2,F3,
COL27 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL28 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL29 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL30 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL31 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL32 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL33 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL34 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL35 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL36 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL37 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL38 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL39 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL40 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL41 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL42 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL43 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL44 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL45 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL46 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL47 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL48 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL49 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL50 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL51 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
COL52 found 80 defective pixels:ROW1F1,FD1,F2,FD2,F3,FD3
*************************************************************
TOTAL NUMBER OF DEFECTIVE PIXELS = 2271 from 4160
*************************************************************
```

```
*************************************************
REPORTING DEFECTIVE PIXELS ON EACH COLUMN
*************************************************
COL7 found 80 defective pixels:ROW1N1,ROW2N1,ROW3N1,
COL8 found 80 defective pixels:ROW1N1,ROW2N1,ROW3N1,
COL25 found 80 defective pixels:ROW1N1,ROW2N1,ROW3N1
COL26 found 80 defective pixels:ROW1N1,ROW2N1,ROW3N1
TOTAL NUMBER OF DEFECTIVE PIXELS = 320 from 4160
```

Wafer K7MWH6T PSI vs. FNAL test results

PSI46V2 K7MWH6T/1 14A



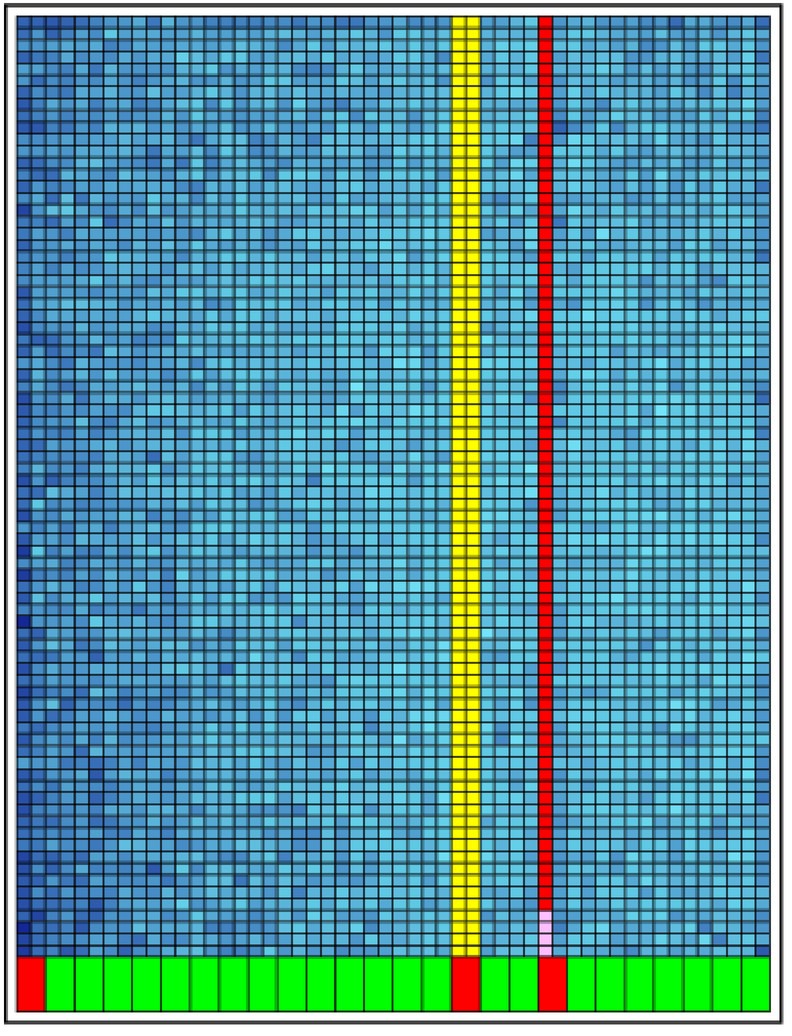
- This is chip A54 for us.
- PSI wafer map report say >= 30 pixels defect (?)
- FNAL shows 2 columns plus 3 more pixels defect
- The agreement between tests is questionable here

```
*********************************************************
REPORTING DEFECTIVE PIXELS ON EACH COLUMN
*********************************************************
COL1 found 1 defective pixels:ROW45N1,N2,N3,
COL6 found 2 defective pixels:ROW67L3A2,ROW70L2A2,
COL21 found 80 defective pixels:ROW1N1,N2,N3,ROW2N1,N2,N3
COL22 found 80 defective pixels:ROW1N1,N2,N3,ROW2N1,N2,N3
*********************************************************
TOTAL NUMBER OF DEFECTIVE PIXELS = 163 from 4160
*********************************************************
```

- Then, chip A53 is a short in both PSI and FNAL report (we measured Idig=92mA)

Wafer K7MWH6T PSI vs. FNAL test results

PSI46V2 K7MWH6T/1 12A



- This is chip A52 for us.
- PSI wafer map report say 2…4 dcol defect (?)
- FNAL shows only 2 pixels defect (wrong address levels)
- We disagree completely here

```
**********************************************************
REPORTING DEFECTIVE PIXELS ON EACH COLUMN
**********************************************************
COL45 found 1 defective pixels:ROW22L1A0,L2A0,L3A0,
COL46 found 1 defective pixels:ROW22L1A0,L2A0,L3A0,
**********************************************************
TOTAL NUMBER OF DEFECTIVE PIXELS = 2 from 4160
**********************************************************
```

- Retesting the chip, with different settings, give us almost the same result
- Conclusion is that we disagree complete here

```
***************************************************
REPORTING DEFECTIVE PIXELS ON EACH COLUMN
***************************************************
COL5 found 1 defective pixels:ROW49N1,
COL45 found 1 defective pixels:ROW22L1A0,
COL46 found 1 defective pixels:ROW22L1A0,
TOTAL NUMBER OF DEFECTIVE PIXELS = 3 from 4160
```